High Gain Ultra-low NF Wideband CMOS Low Noise Amplifier Design using 2-Stage Series-Parallel LC Matching Network

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***Abstract*—The focus of this work is the development of a sub-6 GHz (2-6 GHz) low noise amplifier (LNA) for 5G applications, using a 65 nm CMOS process. A novel two stage common source (CS) cascode source degeneration LNA topology by incorporating a contemporary series parallel LC network and two stage LC network for input and output matching respectively is proposed. The circuit implementation, simulations and evaluation of the LNA's performance are done utilizing the RF Spectre Cadence Virtuoso. According to the evaluation results, the LNA dissipates a total power of 19.6 mW at the supply voltage of 0.7 V. It offers an operational wide bandwidth (BW) of 3.2 GHz which ranges from 2.8 GHz to 6 GHz. The LNA has a peak gain of 36 dB and minimum noise figure (NF) of 1.1 dB across the sub-6 GHz spectrum. The proposed LNA also performs well in terms of stability and linearity measures. The layout of the proposed LNA occupies an area of $0.182mm^2$.**

***Index Terms*—Sub-6 GHz, Millimeter Wave, LNA, 5G Communication, CMOS, 65 nm.**

I. Introduction

5G is the latest international wireless standard, developed to connect a wide range of devices and objects, including machines and other non-human entities. Unlike its predecessors, 2G, 3G, and 4G, 5G operates in both millimeter wave (mm-Wave) and sub-6 GHz frequencies, offering high capacity, multi-gigabit throughput, and low latency. This technology is mainly used to enhance mobile broadband, mission-critical communications, and massive IoTs. Though mm-Wave provide high speeds it does not provide good covereage, sub-6 GHz wireless communication has gained a lot of attention due to its ability to provide greater speed and coverage. Wideband communication systems are particularly interesting because they offer large data rates and fast connectivity. Despite the higher working frequency of 5G, achieving a low NF is preferred to ensure better sensitivity. The focus of this research is on designing a sub-6 GHz receiver, specifically a LNA. The goal is to develop a new wideband LNA that offers high gain, low NF as low as sub-2 dB along with improved performance compared to existing LNAs.

It can be observed that the majority of the designs are classified as either single ended or fully differential, but they have relatively low gain and high NF. By utilizing multiple stages, the initial stage can be enhanced for minimal noise generation and better gain, while the latter stages can be optimized for maximum linearity, there are some recent works on such designs. Common gate (CG) shunt feedback topology is used in [1], [10]. Shunt feedback is used to accomplish the requisite input matching, and series peaking at the input increases the bandwidth of the LNA, but it suffers from high NF because of CG topology. In [6]-[9], a two stage structure with gate inductor-assisted impedance matching procedure and current re-use feed-forward noise cancellation procedure are used to achieve wideband matching, because of noise cancellation topology the gain obtained is low, and NF is also as high as 6 dB. Another work on wideband LNA [5], which has a two-staged configuration that includes a current-mirror with inductive series-peaking for tuned current, this is differential structure, it suffers with low gain and reduced input matching of over 1 GHz. To overcome the problem of low gain and high NF, this work propose a novel design of two stage CS cascode

source degeneration LNA topology by incorporating a contemporary series parallel LC network and two stage LC network for input and output matching respectively. Instead of using buffer stage at the output which is generally used, a two stages of CS cascode structure is used which improves gain and CS degeneration helps in reducing the NF. An external matching networks is employed to achieve 50 Ω constraints.

The following outlines the way the paper is structured. Section II discusses wideband LNA design theory. Section III examines the layout of the LNA and also discusses the pre and post layout simulation findings. Section IV draws the conclusion to the work.

II. Design and Analysis

In the LNA design, optimizaton of numerous aspects including gain, linearity, NF, power consumption, input and output matching. An LNA's performance metrics are linked. So, improving one of them deteriorates the other one. As a result, building an LNA includes refining all of them or adopting any strategy to reduce the compromise between those figures.

A. Proposed LNA

In this proposed design a two stage CS cascode source degeneration LNA topology is used and enhanced by incorporating a contemporary series parallel LC network and two stage LC network for input and output matching respectively as shown in Fig. 1. Instead of using buffer stage at the output which is generally used, a two stage CS cascode structure is employed here.

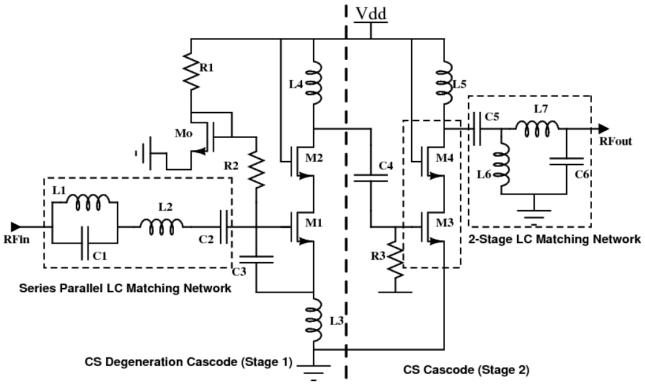

Fig. 1. Schematic Design of LNA.

1) Schematic Analysis: In contrast to the general two stage structure which uses buffer output stage, this work proposes use of the same CS cascode stage to improve gain. In a general CS cascode topology in order to enhance the gain at lower frequencies a resistive network is used at the drain of the cascode amplifier but it reduces the headroom for maintaining the transistors in the cascode structure to operate in saturation region. Since this work uses a two stage amplification the gain at lower frequencies is taken care, so in order to eliminate the headroom problem the resistor R_L at the drain of the cascode transistor can be removed, the purpose of inductors is to regulate the gain at higher frequencies and also for obtaining better matching response at the output. A parallel LC circuit of inductor L_1, capacitor C_1 is connected in series with a series LC arrangement which contains inductor L_2, capacitor C_2 is presented just at the input of the CS degeneration cascode topology in our design. Because the LNA's input impedance comprises of a reactive impedance, a combination of reactive elements L_1, L_2, C_1 and C_2 are used which aids in resonance of the network with input reactance over the desired spectrum, resulting in good input matching and increased band of operation. The capacitance C_3, which is in parallel with C_{gs} of the transistor M_1, contributes to increase in the bandwidth. The cascade arrangement of the transistors M_1 and M_2 enhances the amplifier input to output reverse separation and frequency response.

2) Input and Output Matching: The transistor M_1 has an input impedance which is a parallel LC combination in series with an series LC combination, as shown in the circuit, and is given by:

$$\mathrm{Z_{in}} = \mathrm{s(L_2{+}L_3)}{+}\frac{1}{s.\mathrm{C_2}}{+}\frac{1}{s.\mathrm{C_3}}{+}\frac{\mathrm{g_{m1}L_3}}{\mathrm{C_3}}{+}\frac{\mathrm{L_1}}{\mathrm{C_1}}\left(\frac{1}{\mathrm{sL_1}+\frac{1}{\mathrm{sC_1}}}\right) \quad (1)$$

The real segment of input impedance should be matched with the source resistance offered in the circuit to achieve good input impedance matching. The bandwidth is determined by the reactive elements used in the filter. The input return loss indicated by S_{11} is an accurate indicator of input matching. The lower the value, the better the input match. For the output matching the 2-stage-LC network is used to transform the output impedance to 50 Ω. The combined impedance of C_5, L_5, L_6, L_7 and C_6 achieves the desired wideband impedance match.

3) Gain Analysis: The target is to attain a sufficiently higher gain across desired spectrum. The proposed LNA's high gain is primarily due to the two identical CS cascode stages as shown in Figure 4.3.1. The power dissipated, however, remains close to that of a single stage design. The total voltage gain is calculated by multiplying the gains of individual stages of the LNA as:

$$\mathrm{A_v} = \mathrm{A_{v1}} \times \mathrm{A_{v2}} \quad (2)$$

The main transistor, M_1, is biased by a separate current mirror circuitry comprising of MOSFET M_0, the cascoded transistors in both first and second stage that is transistors M_2 and M_4 respectively are biased using V_{dd} supply. A cascode pair delivers high gain while retaining strong reverse separation. The identical cascode second stage is added to boost the total gain even more. Furthermore, this stage completely separates the LNA's input and output matching. To deliver accurate supply voltage to the caccode transistors at both the stages, M_2 and M_4 Inductors, L_5 and L_4, are

placed at the drain.

4) Noise Analysis: The first stage's NF dominates total NF in the two-staged wideband LNA. Furthermore, the higher the first stage's gain, the lower the noise contribution of the subsequent stage. This corresponds to the Friis formula, which is as follows:

$$\mathrm{F} = \mathrm{F}_1 + \frac{\mathrm{F}_2 - 1}{\mathrm{G}_1} \tag{3}$$

Where F represents the total noise factor, F_1 and F_2 represent the first and subsequent stages of noise factors, whereas G_1 indicates the first stage gain. Since the impact of the subsequent stage's noise factor is reduced because of the large gain of the initial stage, the principal noise sources are drain current noise, gate-induced noise generated by the cascode stage (M_1 and M_2), and thermal noise generated by the resistor. From dc biasing, V_{dd} is 0.7 V. Also the average current (I_{avg}) is 27.8 mA. Therefore, power consumption is calculated as:

$$\text{Power consumed} = P_d = I_{avg} * V_{dd} = 19.46 \text{ mW} \tag{4}$$

The optimal NF of proposed LNA can be expressed as:

$$F_{opt} = 1 + \frac{2\gamma}{\alpha} * (\frac{\omega_0}{\omega_T}) * \sqrt{p}(|c| + \sqrt{p} + \sqrt{1+p}) \tag{5}$$

where p is technology parameter dependent on the CMOS technology parameters δ, α and γ, and is formulated as $\frac{\delta.\alpha^2}{5.\gamma}$. By taking c as 0.4, δ which is normally equal to 4, α is taken to be 0.9, γ which is taken as 2. The value of p is 0.147. So, F_{opt} is calculated as:

$$F_{opt} = 1 + \frac{4}{0.9}.(\frac{4e^9}{2.77.e^{11}}).\sqrt{.147}.(0.4 + \sqrt{.147} + \sqrt{1 + .147})$$

$$F_{opt} = 1 + 0.2872 = 1.2872$$

$$Noise\ \ figure\ \ (dB) = 1.2872 = 10log(1.2872) = 1.1\ \ dB$$

The stability of the LNA is determined by two parameters K_f and B_{1f}, which are evaluated as:

$$K = \frac{1 - |S_{21}|^2|S_{11}|^2 + B_{1f}^2}{2 * |S_{12}S_{21}|} \tag{6}$$

$$B_{1f} = |S_{11}||S_{22}| - |S_{21}||S_{12}| \tag{7}$$

If $K_f > 1$ and $B_{1f} > 0$ then the circuit is unconditionally stable. Simulated values of K_f and B_{1f} obtained at 4 GHz respectively are 92.981 and 1.011. The figure of merit of the proposed LNA is evaluated as:

$$FOM = \frac{S_{21}, maxXBandwidth[GHz]}{(NF, min - 1)XP_d[mW]} \tag{8}$$

For Sub-6 GHz band (2-6 GHz) the bandwidth is 4 GHz, simulated bandwidth by considering range where S_{11} is less than -10 dB is (2.8-6 GHz) = 3.2 GHz.

$$FOM = \frac{36X3.2}{(1.1 - 1)X19.56} = 58.89$$

III. Results and Discussion

The proposed LNA is built in a low leakage 65 nm CMOS technology. The inductors in the design are implemented using RF spiral symmetrical inductors, while the capacitance is achieved through the utilization of low leakage metal-insulator-metal capacitors. All gate bias resistors and feedback resistors are implemented using n^+ poly resistors. The MOSFETs utilized in the design are 65 nm low leakage low threshold RF transistors. Layout is drawn using Layout-GXL suite in the Cadence Virtuoso. Assura tool has been used for layout verification. DRC rule checks, LVS and parasitic extraction using generated Assura have been found successful. The Fig. 2 shows the layout of the proposed design.

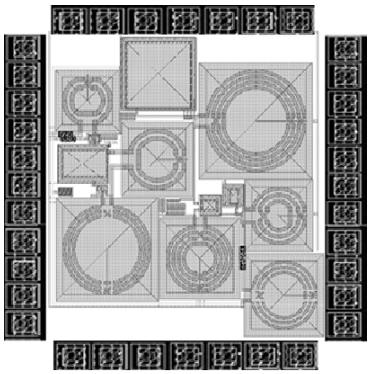

Fig. 2. Layout of the Proposed Design.

Post layout simulations are performed to check the effects of parasitic elements on the designed LNA. The layout is optmized in several ways by tuning the sizes of metal interconnects, placement of each design element in the proposed design. The layout of the designed LNA which occupied an area of 0.182 mm^2.

All the performance analysis and results have been obtained using the Cadence Virtuoso ADE-L design and simulation environment. S-parameter simulation is done for obtaining the noise performance, stability performance, gain analysis and matching network quality. Pss analysis is for checking the linearity measures P_{1dB} and IIP3. Final tuned values of values of the design components is shown in Table I.

TABLE I
Component sizes of LNA

Component	Description
Transistor Width	M_1=49 μm, M_2=48 μm, M_3=48 μm, M_4=24 μm and M_5=4 μm
Transistor Length	All are 65 nm
Resistors	R_1 =1.8 KΩ, R_2=50 KΩ, R_3=50 KΩ
Capacitors	C_1=51.16 fF, C_2=6.22 pF, C_3=51.16 fF, C_4=20 pF, C_5=1.04 pF and C_5=1.04 pF
Inductors	L_1=1.658 pH, L_2=357 pH, L_3=244 pH, L_4=2.99 nH, L_5= 1.18 nH, L_3=985 pH and L_3=540 pH
Supply Voltage	700 mV

All the S-parameters simulation results for both pre and post layout work are performed. As observed in Fig.

3, proposed design is able to achieve a peak gain (S_{21}) of 36 dB as well as an overall gain of above 15 dB. It can also be observed that the design achieved fairly good input matching which is indicated by input return loss (S_{11}) curve less than -10 dB from 2.8 GHz to 6 GHz. The best input match is happening at 4.7 GHz which is -18 dB. Fig. 4. shows the reverse transmission (S_{12}) and output matching (S_{22}) which are less than -10 dB and -70 dB respectively. The best figure for S_{12} and (S_{22}) in the entire band are -40 dB and -97 dB respectively. Fig. 5. shows the NF response in the band of interest, the minimum NF obtained is 1.1 dB and maximum NF obtained is 2.5 dB. Fig. 6. shows the input impedance matching, it can be observed that the proposed design is able to match the impedance around 30 Ω to 50 Ω in the frequency range 2.5GHz to 6 GHz, which is very good for the maximum power transfer and minimum power reflection.

The linearity parameter simulation is performed. Fig. 7. shows the third order intercept point it can be seen that IIP3 obtained is -16.54 dBm at 4 GHz frequency, also the deduced input referred P_{1dB} at 4 GHz is -25.73 dBm, this verifies the relatioship between the 1 dB compression point and IIP3 that is the difference has to be approximately between -9.6 dBm to 11 dBm. Fig. 8. shows the stability curves, for unconditional stability B_{1f} must be > 0, and K_f must be > 1, it can be observe that the design is able to achieve the above mentioned criterion in the entire frequency band of interest thus our design is unconditionally stable. The broadband LNA designed in 65 nm CMOS process which dissipates a total of 19.56 mW power from 0.7 V supply. This LNA achieved a very good FOM of 58.89. Occupying an area of $0.182mm^2$.

The Table II provides the comparison for the proposed design with various recent works in sub-6 GHz for 5G Applications. FOM indicates the quality of design by considering all the performace parameters. Higher the FOM it can be claimed that the design is better. It has been observed that the FOM of our design is 58.89 which is very good figure.

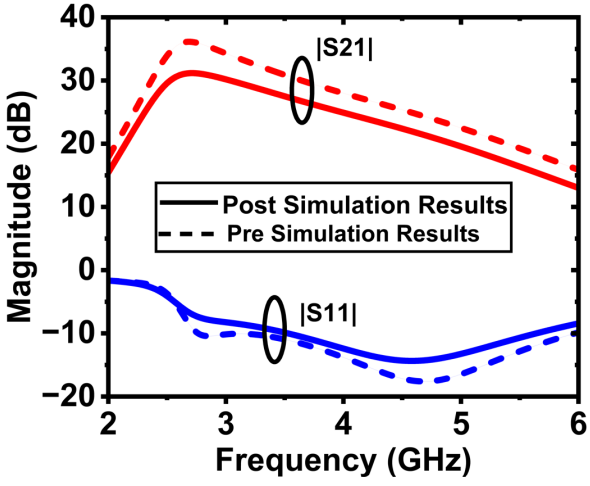

Fig. 3. Gain & Input Return Loss vs Frequency.

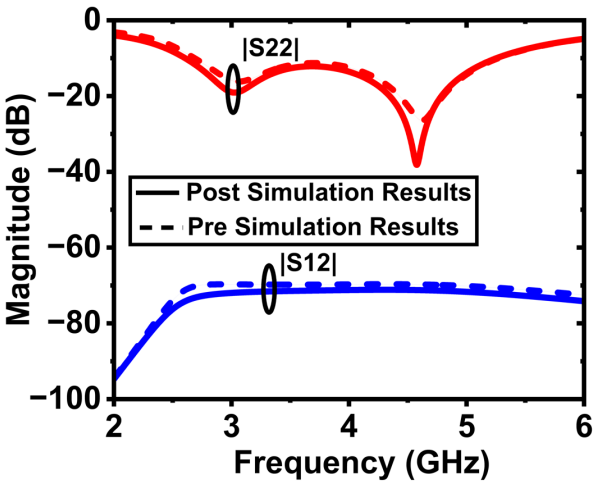

Fig. 4. Reverse Transmission & Output Return Loss vs Frequency.

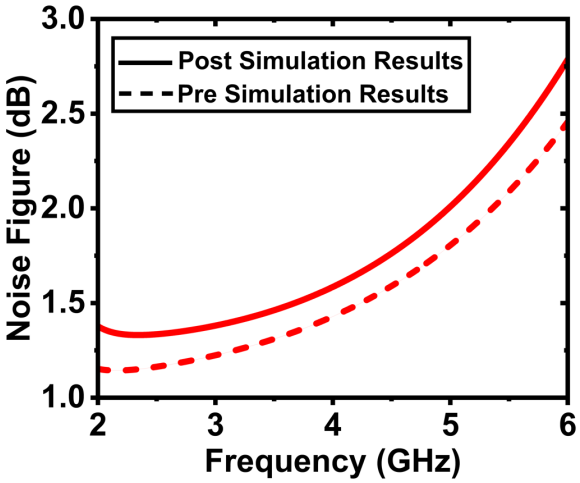

Fig. 5. Noise Figure vs Frequency.

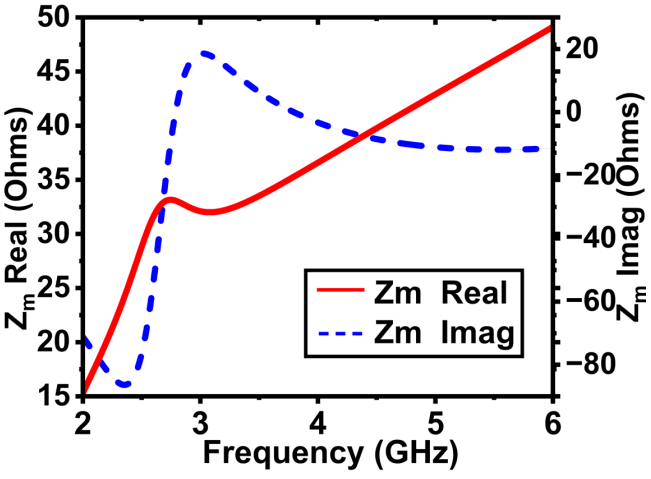

Fig. 6. .Input Impedance Matching vs Frequency.

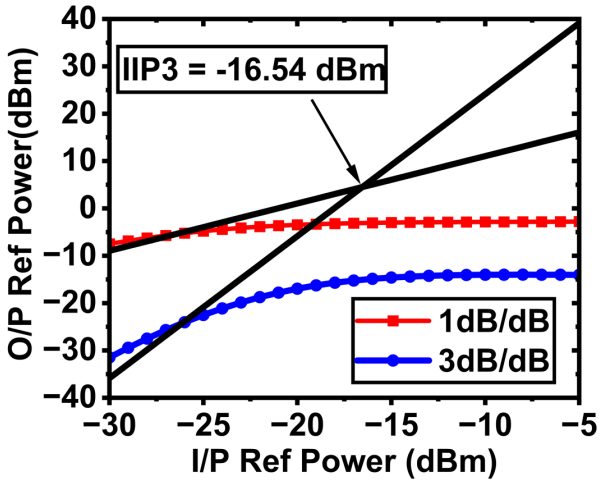

Fig. 7. IIP3 Curve at 4G.

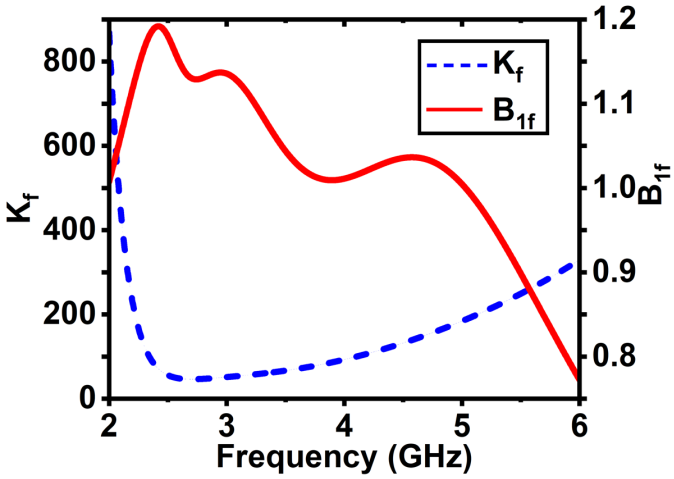

Fig. 8. Stability vs Frequency.

TABLE II
COMPARISON OF PROPOSED LNA WITH OTHER WORKS

References	This Work	[4]	[2]	[3]	[11]
Process	65 nm CMOS	130 nm CMOS	180 nm CMOS	180 nm CMOS	130 nm CMOS
Topology	2-Stage (IDCS Cascode)	2-Stage (IDCS Cascode)	CG with g_m-enhancement	current-reuse-noise cancellation	Differential CCC-CG
Bandwidth (GHz)	2.8 - 6	4 - 6	0.5 - 3.5	2 - 5	3.5 - 7
S_{21} (dB)	36 (peak gain)	25.5 (peak gain)	15.7 (peak gain)	13 (peak gain)	24 (peak gain)
NF (dB)	1.1	1.9	3.2	6	2.8
Power dissipation	19.46 mW	20.9 mW	1.4 mW	1.8 mW	2.4 mW
FOM	58.89	NR	23.11	3.6	NR
IIP3 (dBm)	-16.54	-13.47	-2.8	NR	-0.33
1-dB compression point (dBm)	-25.73	-25.07	NR	-15	NR
Area in mm^2	0.182	1.26	0.35	0.72	0.24

*NR indicate No Result.

*More FOM indicates better design.

* $FOM = \frac{S_{21},maxXBandwidth[GHz]}{(NF,min-1)XP_d[mW]}$.

IV. Conclusion

The broadband LNA designed in 65 nm CMOS process for sub-6 GHz band which dissipates a total of 19.56 mW power from 0.7 V supply. Proposed a new design by incorporating novel techniques such as series parallel LC input matching network, 2-stage LC output matching network and a two stage CS cascode LNA topology. This work achieved good peak gain of 36 dB, lowest noise figure of 1.1 dB and covering bandwidth from 2.8 GHz to 6 GHz covering the sub-6 GHz band of the electromagnetic spectrum. The LNA of this work has a good FOM of 58.89 compared to other broadband LNAs. The design could also able to get a good reflection coefficient S_{11} of less than -10dB and stability over entire range of frequency. The layout is generated and verified using the Cadence Virtuoso. Assura tool used for DRC rules and LVS which is found correct and matched with schematic. The total area occupied by the LNA is 0.182 mm^2.

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