Passive 5.8GHz RF Energy Harvester in 65nm CMOS

Aristotle D. Lopez, *Member, IEEE*, and Louis P. Alarcón, *Member, IEEE*

***Abstract*— This paper presents a passive 5.8GHz RF Energy Harvester (RFEH) implemented in 65nm CMOS technology that allows batteryless operation and reduction in overall size of WSN and IoT sensor nodes, which are limiting more widespread implementation. The RFEH consists of an on-chip matching network and optimized rectifier that are co-designed for maximum efficiency and sensitivity in the RFEH in gathering the required energy for the load circuit. The passive 5.8GHz RFEH prototype demonstrated a sensitivity of around -13dBm in gathering enough energy to produce 0.5V on a 10uF capacitive load, allowing the harvested energy to be reasonably combined with energy from other sources. When used as the only energy source, the ability to gather and provide a continuous supply of 8uW (10uA at 0.8V) is demonstrated, which is enough to power low-power RF circuits such as OOK and FSK receivers without the need of any battery, allowing batteryless operation.**

***Index Terms*— RF Energy Harvesting, Batteryless, IoT.**

I. Introduction

Wireless Sensor Networks (WSN) and Internet of Things (IoT) are technologies that enable monitoring of physical and environmental conditions. Recent research has focused on making the sensors more autonomous, allowing them to be easily deployed in any environment, requiring minimal maintenance. One of the main impediments in achieving autonomous operation is the limited supply of power available to the sensor node. Typical implementations use batteries that are bulky and have a finite lifetime. Batteries limit the reduction of size and the cost of implementation of these sensor nodes. Energy harvesting, wherein the energy needed by the sensor is gathered from the environment, is a possible solution to this problem. If enough energy were obtained from the environment, energy storage using batteries would be unnecessary and can be removed.

It is desirable to gather as much energy from the environment as possible. A Multimode Energy Harvesting System, where energy from multiple sources are combined, is advantageous [1]. RF is a desirable energy source because of its widespread use. However, its limited energy density is making it hard to be combined with other higher density energy sources. Developing a RF Energy Harvester that has higher sensitivity and efficiency will make it more practical to use as energy source. Other developments that are making autonomous operation more feasible are related to reducing the power requirement of sensor nodes. Recent research show RF wakeup receivers that can operate with a 37nW, 0.54V supply [2], BLE receivers that operate using 236nW[3], and 370 pJ/bit BFSK/QPSK Transmitters.[4] With these low energy requirements, RF as the only energy source is becoming more feasible.

Recent survey show most RF Energy Harvesters are operating at frequency bands of 900MHz and 2.4GHz [5]. This is limiting the size reduction of sensor nodes because at these frequencies, RF components such as antenna needs to be large. Moving to a higher operating frequency bands such as 5.8GHz is required to reduce the dimension of these components. Most RF Energy Harvesters operating at 5.8GHz use discrete Schottky diodes, which again prevents reduction of sensor node size. Having a 5.8GHz RF Energy Harvester that is implemented on silicon and can be packaged with the other circuits of the sensor nodes on a chip is very useful in achieving more autonomous WSN and IoT.

II. Energy Harvesting System

An implementation of the Multimode Energy Harvesting is shown in Fig. 1. Each energy source will have a local storage capacitor (C_{RF}, C_{PL}) where they independently store their gathered energy. To be able to combine the energy from higher energy density source (Powerline) to a lower energy density source (RF), the energy combination can be time-multiplexed. A controller can schedule the "transfer" of the locally gathered energy to a main storage capacitor (C_{MAIN}), which then will supply energy requirement of load circuits. For this mechanism to be practical, RF Energy Harvester needs to have maximum sensitivity and efficiency to gather and store enough energy on its local storage capacitor within a target duration. If RF is the only available energy source, then the controller should be able to monitor the local storage capacitor, C_{RF} and transfer energy to C_{MAIN} once enough energy is gathered.

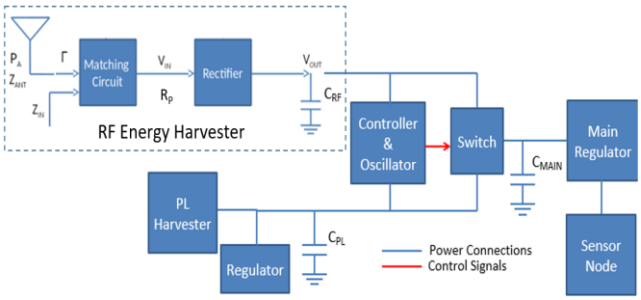

Figure 1. Multimode Energy Harvesting (PL, RF)

A. RF Energy Harvesting

The RF Energy Harvester (RFEH) converts RF energy to DC and is composed of the antenna, matching network, rectifier, and storage capacitor as shown in Fig. 1. The antenna gathers the RF energy from the environment and provides the input power (P_A) available for energy conversion to the matching network. The matching network matches the antenna impedance to the input impedance of the rectifier and transfers the RF signal from the antenna to the rectifier. The level of matching, measured by the reflection coefficient (Γ), determines the percentage of the input power that is transferred to the rectifier. The voltage gain of the matching network is the ratio of the input voltage

A. D. Lopez and L. P. Alarcón are with the Microelectronics and Microprocessors Laboratory, Electrical and Electronics Engineering Institute, University of the Philippines - Diliman, Quezon City, Philippines 1101 (e-mail: aristotle.lopez@upd.edu.ph; louis.alarcon@eee.upd.edu.ph)

from the antenna and output voltage provided to the rectifier. Together with the equivalent load resistance of the rectifier (R_P), the design of the matching network determines the voltage gain and needs to be maximized for higher sensitivity. Thus, the matching network controls the input voltage (V_{IN}) and the input power (P_{IN}) that is available as the rectifier input.

The rectifier converts the input signal it receives from the matching network to DC power (rectification) and multiply the voltage level (voltage multiplication) to increase the output voltage (V_{OUT}) to the required level, within the required charging time in the load capacitor. Properly designing the rectifier to minimize losses and maximize its input resistance, determines the sensitivity and efficiency of the RFEH. The matching network and rectifier performance affects each other and they need to be designed together to maximize sensitivity and efficiency. The load capacitor, C_{RF} stores the harvested energy before transfer to the succeeding load circuits. This capacitor needs to be optimized based on system requirements.

B. Sensitivity

The sensitivity of a RF Energy Harvester is commonly defined as the minimum P_A needed to turn-on the RF Energy Harvester (RFEH) and start gathering energy. However, in a practical multi-mode RFEH system, there is time limit for each of the energy harvesters to gather the required energy. In a RF Energy Harvester, a P_A that barely turn-on the rectifier would take a large amount of time to gather the required energy and is not very useful. This minimum P_A is not a practical measure of sensitivity. For this study, the sensitivity is the minimum operating range of the RF Energy Harvester is defined as the minimum P_A that would allow gathering of the required energy and store that energy on a storage capacitor within a limited amount of time required by the energy harvesting system.

For a multi-mode EH system with fixed capacitive load, the energy gathered and stored is $\frac{1}{2}C_{LOAD}V_{OUT}^2$. Where C_{LOAD} is the capacitance of the load and V_{OUT} is the voltage at the load. Since C_{LOAD} is fixed, the energy is determined from the V_{OUT}. For a RF Energy Harvester with capacitive load, the minimum sensitivity can be defined as minimum P_A that will produce a target V_{OUT} on a capacitive load. This voltage can be monitored by the controller to determine if enough energy has been gathered.

C. Efficiency

In a RF energy harvester with capacitive load, the efficiency is determined by the charging time, T_C in producing a fixed output voltage, $V_{OUT}(T_C)$ at the storage capacitor as described by (1) and (2). The faster the charging time, the higher the amount of charge that is being transferred to the storage capacitor per cycle, and the higher the output power. For a fixed input power level, the faster the charging time, the higher the efficiency. Losses in the RF energy harvester reduces the amount of charge transferred to the output per cycle, thus increasing the charging time and reducing the efficiency. The RFEH is designed to minimize T_C to maximize efficiency.

$$\eta_{RFEH} = \frac{P_{OUT}}{P_A} \tag{1}$$

$$P_{OUT} = \frac{{}^1\!/_2 C_{OUT}(V_{OUT}(T_C)^2 - (V_{IN} - V_{DROP})^2)}{T_C} \tag{2}$$

III. Matching Network

The matching network matches the antenna to the rectifier and provides voltage gain in producing an input voltage (V_{IN}) to the rectifier. The level of matching, measured by the reflection coefficient (Γ), and the input impedance (Z_{IN}) affects the level of V_{IN} [7] as described in (3). Higher Zin would produce higher V_{IN} but would result in more losses due to mismatch. The matching network needs to be designed properly to be able to minimize reflections but produce enough minimum V_{IN} to the rectifier. This way the maximum efficiency can be produced at the required V_{OUT}.

$$V_{IN} = \sqrt{(1 - \Gamma^2) \cdot 2 \cdot P_A \cdot Z_{IN}} \tag{3}$$

The voltage gain in the matching network is defined as the ratio of the antenna voltage, V_A to the output voltage in the matching network, which is the same as the input voltage to the rectifier, V_{IN}. Maximizing the voltage gain results in a lower P_A required to produce the required V_{IN} in the rectifier, maximizing sensitivity. The voltage gain is also dependent on the load, which is the input impedance of the rectifier [10]. The voltage gain can be approximated by (4), where $R_S + jX_S$ is the series input impedance of the rectifier. To maximize the voltage gain, R_S needs to be minimized while X_S needs to be maximized. To minimize losses in the matching network and increase efficiency, it is desired to use high Q components and minimize number components. Thus, it is desirable to use a single-stage matching network.

$$G_{MN} = \frac{X_S}{R_A + R_S} \tag{4}$$

At the input of the rectifier, the R_S is expected to be very small, but due to the parasitic inductance and capacitance added by the wirebond and pads at 5.8GHz, the R_S value will be increased. If off-chip components are used in the matching network, the R_S is already high due to the parasitics, resulting in reduced voltage gain. Because of this limitation, it is desired to put the matching network on the chip, as close to the rectifier as possible. This would ensure the lowest R_S value in the load, seen by the matching network and voltage gain would be maximized.

IV. RF Rectifier

A. Rectifier Topology

A popular rectifier topology used is the Dickson topology and is typically implemented with diode-connected transistors. Its turn-on voltage, which is the minimum input voltage that would allow the rectifier to operate, is approximately equal to the threshold voltage of the transistors (V_{TH}) [8], which is typically around 300mV-400mV in 65nm CMOS. This turn-on voltage is higher than the typical input voltage levels expected from RF inputs (200mV from –4dBm P_A), limiting the minimum operating range. Several techniques are used to reduce the V_{TH} levels of the transistors to allow for lower voltage inputs to turn-on the rectifier. One of the most efficient topology is the Cross-Coupled Differential Drive rectifier (CCDD) [9]. In this topology, the V_{TH} is cancelled, allowing for lower V_{TH} and resulting in a lower input voltage requirement and thus improved sensitivity. To produce the required output voltage (V_{OUT}), several of these rectifier cells are cascaded. A graph

showing the RF input voltage (V_{IN}) required to produce 1V DC output voltage is shown in Fig. 2 for the two topologies.

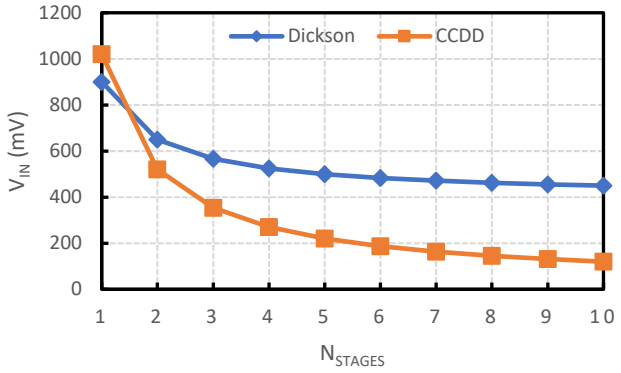

Figure 2. Required V_{IN} for 1V V_{OUT} in Dickson vs. CCDD Topology

It is evident from the graph that the CCDD topology would be able to produce the required V_{OUT} for lower V_{IN} levels, which results in a better sensitivity. Also evident from the graph is the limitation of the Dickson topology at input voltages closer to the threshold voltage of the transistors, where the additional stage does not reduce too much the required V_{IN}. Thus the need to minimize the transistor threshold voltage. Any additional rectifier stages higher than N = 8 contribute mostly losses and minimal voltage multiplication. For an input voltage of 350mV, the Dickson rectifier topology would need more than 10 stages while the CCDD rectifier would only need 3 stages. For low power and low voltage inputs expected from energy sources like RF, the CCDD topology is better because of the lower turn-on voltage and the lesser number of stages needed to produce the required output, which means less components, resulting in less losses incurred and higher efficiency.

B. *Cascaded Rectifier Stages*

In a typical rectifier, the required output voltage is higher than the input voltage. A single rectifier stage will not be able to produce the required output, thus several rectifier stages are cascaded to multiply the voltage produced by a single rectifier stage and be able to produce the required V_{OUT}. The V_{OUT} expected in a cascaded rectifier is described by (5), where V_{IN} is the amplitude of the RF input signal to the rectifier, V_{DROP} is the drop in voltage level due to losses in a rectifier stage, and N is the number of stages included in the rectifier cascade. N affects both the required V_{OUT} and charging time and is critical in determining the sensitivity and efficiency of the RF energy harvester. In the rectifier, a maximum of 2* V_{IN} increase in V_{OUT} per stage is expected. But losses cause a drop in voltage (V_{DROP}) that reduces the voltage produced per stage. The lower the loss, the lower the V_{DROP} and the higher the V_{OUT} produced. V_{IN} is directly proportional to input power level (P_A) while V_{DROP} is dependent on the sizing of the transistors. Minimizing V_{DROP} and increasing N reduces the required V_{IN}, allowing lower input power levels to produce the required output which improves the sensitivity and increases the operating range.

$$V_{OUT} = N \cdot (2 \cdot V_{IN} - V_{DROP}) \quad (5)$$

Fig. 3 illustrates the voltage levels available at the output of each rectifier stage of a 5-stage cascaded rectifier, resulting from a 5.8GHz input signal with amplitude V_{IN}. Each stage contributes around 2Vin - V_{DROP} of additional voltage to the output. For a V_{IN} of 200mV, the output at the 1st stage V1 is around 290mV. Each additional stage contribute an additional voltage equal to the voltage level at V1, showing the voltage multiplication introduced by cascading rectifier stages.

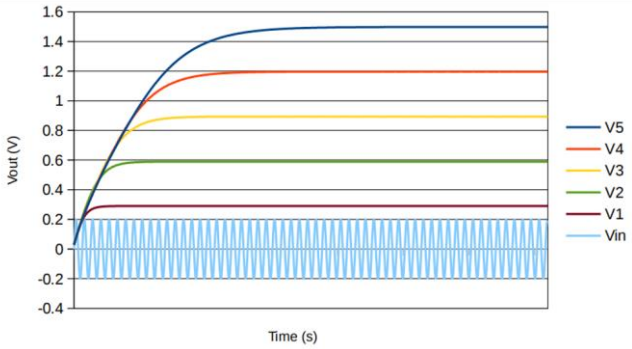

Figure 3. Simulated Rectifier V_{OUT} per Number of Stages, N (V_{IN} = 200mV)

C. *Transistor Sizing*

In CCDD topology, each rectifier stage is composed of switches, which are implemented using PMOS and NMOS transistors and charge pump capacitors. The transistors are normally sized to minimize V_{TH} and increase sensitivity. But minimizing V_{TH} also increases leakage, reducing efficiency. To maximize efficiency in a rectifier, the amount of charge transferred through the switch should be maximized while minimizing leakage of the transfer. The charge transfer happens when the switches are ON and the leakage is encountered when the switches are OFF. The transistors are sized such that the ratio of the ON resistance (R_{ON}) to the OFF resistance (R_{OFF}) is maximized.

D. *Charge-Pump Capacitors*

The charging time of the output from an initial value of $V_{OUT}(0)$ to the target value of $V_{OUT}(T_C)$ can be estimated using (6). The charging time is dependent on the number of stages, N and the charge pump capacitance, C_P. The C_P should be sized together with N [6].

$$T_C = T \cdot \left(N \frac{C_{OUT}}{C_P} + 0.3N + 0.6\right) \cdot \ln\left[\frac{(N+1)\cdot V_{IN} - V_{OUT}(0)}{((N+1)\cdot V_{IN} - V_{OUT}(T_C))}\right] \quad (6)$$

Choosing a capacitance lower than the required C_P value means less charges being transferred to the output than needed, resulting in a higher charging time than required. A higher C_P value would allow more charge to be transferred to the output but higher capacitance values also results in higher leakage values that reduce the charge transferred to the output capacitor and increases charge time. Having C_P values that are not optimum would reduce efficiency, and possibly increase the charging time to above that is required by the system.

E. *Load Impedance*

The load impedance seen by the matching network is the input impedance of the rectifier. For maximum sensitivity, the equivalent parallel load resistance (R_P) of the rectifier seen by the matching network should be maximized. For a multi-stage rectifier however, the equivalent R_P decreases with increasing number of stages, N. This is due to the contribution of the additional switches and capacitances as N is increased, requiring additional current. This reduces the

voltage gain available in the matching network as shown in Fig. 4. The voltage multiplication available from increasing N in the rectifier can reduce the voltage gain provided by the matching network. Thus, increasing N has a cost in V_{IN}, which ultimately might reduce V_{OUT}.

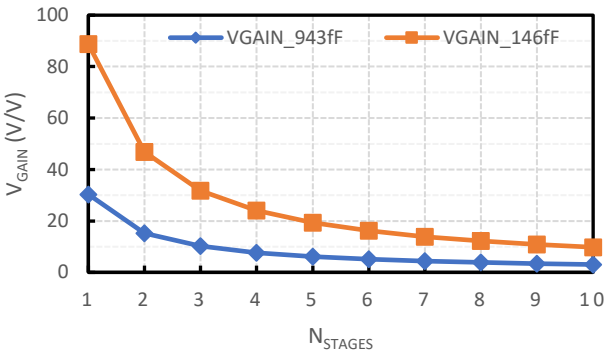

Figure 4. Matching Network Voltage Gain per Number of Stages, N

In designing the rectifier, N should be minimized for a target V_{OUT} to maximize voltage gain in the matching network and improving overall sensitivity. Also evident is the need for the matching network and rectifier to be optimized together as the design that improves the rectifier, sometimes degrades the performance of the matching network.

V. Measurement Results

The design considerations described above were used to implement a RF Energy Harvester (RFEH) in 65nm CMOS technology to be able to harvest energy from a 5.8GHz input and store the energy on a 10uF load capacitor. The circuit consists of a 3-Stage CCDD rectifier with on-chip single-stage pi-matching network as shown in Fig. 5.

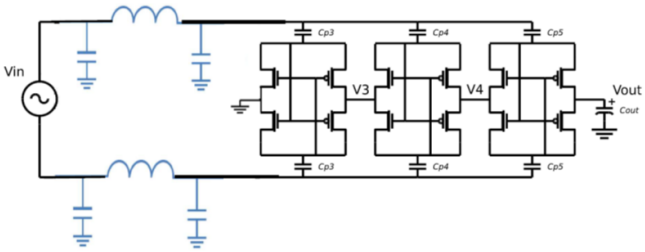

Figure 5. 5.8GHz RF Energy Harvester Circuit Diagram

The test setup for the characterization is shown in Fig. 6, where a RF Signal Generator provide a 5.8GHz input and a Source Meter Unit measures the resulting DC output.

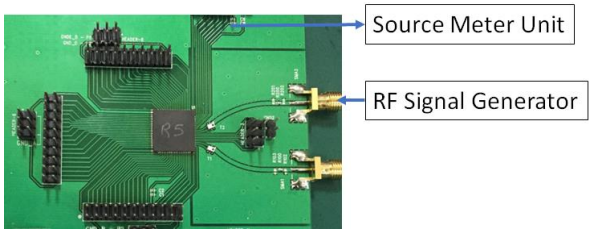

Figure 6. Characterization Test Setup

Test results shown in Fig. 7 show that a RF Energy Harvester has a sensitivity of around -13dBm in gathering 3uJ DC energy, able to produce a 0.5V on a 10uF C_{LOAD} from a 5.8GHz input. The sensitivity of the testchip is around 6dB worse than simulated results.

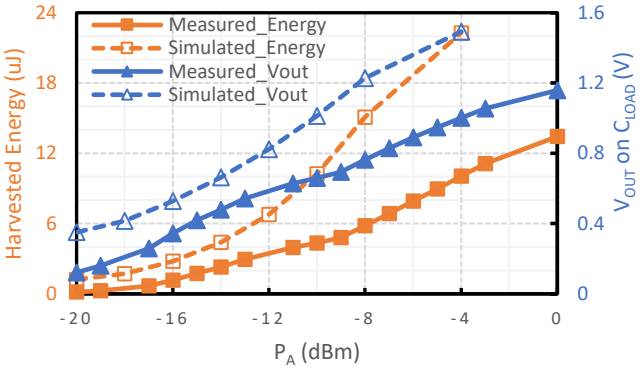

Figure 7. RF to DC Energy Conversion (Simulated vs Measured)

Test results in Fig. 8 show that with an -8dBm (~210mV V_{IN}), 5.8GHz input, the RF Energy Harvester can gather and store enough energy to produce 0.8V on a 10uF load capacitor within 2s. This makes the RFEH practical to combine its harvested energy with a higher energy density in a Multimode Energy Harvesting System.

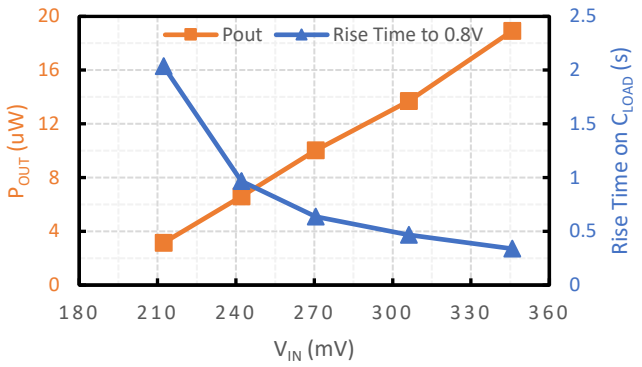

Figure 8. P_{OUT}, V_{IN}, and Rise Time to 0.8V for P_{IN} = -8dBm to -3dBm

In Fig. 9 below, test results show that the RF Energy Harvester can provide a continuous 8uW (10uA, 0.8V) supply when harvesting energy from a 5.8GHz, -4dBm input, more than enough to power recent low power circuits.

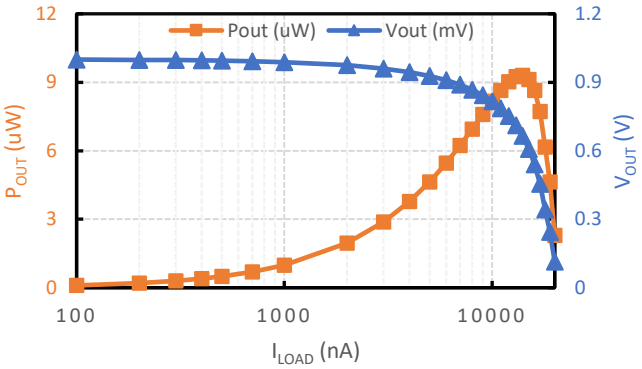

Figure 9. RFEH Performance vs Continuous Current Load

VI. Conclusion

This study presented the practical design considerations in the co-design of the rectifier and matching network of a passive 5.8GHz RF Energy Harvester (RFEH) for

maximum sensitivity and efficiency. To achieve this, the design of the rectifier and matching network are optimized together to provide maximum voltage gain in the RFEH for the required output level. Without requiring another power supply, the passive 5.8GHz RFEH prototype implemented in 65nm CMOS technology, demonstrated a sensitivity of around -13dBm in gathering 3uJ DC energy, enough to produce 0.5V on a 10uF capacitive load. If used as the only energy source, the prototype also demonstrated the ability to gather and provide a continuous supply of 8uW (10uA at 0.8V), which is enough to power low-power RF circuits such as OOK and FSK receivers without the need of any battery, allowing batteryless operation. The reduction of circuit dimensions due to higher frequency of operation also allows the RFEH to be incorporated together with other blocks of a sensor on a single chip. This passive 5.8GHz RFEH results in smaller, cheaper, more practical IoT and WSN sensor nodes that enables autonomous operation.

ACKNOWLEDGMENT

This research would not have been possible without the support and funding of the CHED-PCARI project, the DOST-ERDT project, and DOST-PCIEERD.

REFERENCES

[1] A. Wang, J. Kwong and A. Chandrakasan, "Out of Thin Air: Energy Scavenging and the Path to Ultralow-Voltage Operation," in *IEEE Solid-State Circuits Magazine*, vol. 4, no. 2, pp. 38-42, Spring 2012.

[2] V. Mangal and P. R. Kinget, "Sub-nW Wake-Up Receivers With Gate-Biased Self-Mixers and Time-Encoded Signal Processing," in *IEEE Journal of Solid-State Circuits*, vol. 54, no. 12, pp. 3513-3524, Dec. 2019.

[3] N. E. Roberts et al., "26.8 A 236nW −56.5dBm-sensitivity bluetooth low-energy wakeup receiver with energy harvesting in 65nm CMOS," *2016 IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, USA, 2016, pp. 450-451.

[4] K. -H. Teng and C. -H. Heng, "A 370-pJ/b Multichannel BFSK/QPSK Transmitter Using Injection-Locked Fractional-N Synthesizer for Wireless Biotelemetry Devices," in *IEEE Journal of Solid-State Circuits*, vol. 52, no. 3, pp. 867-880, March 2017.

[5] C. R. Valenta and G. D. Durgin, "Harvesting Wireless Power: Survey of Energy-Harvester Conversion Efficiency in Far-Field, Wireless Power Transfer Systems," in *IEEE Microwave Magazine*, vol. 15, no. 4, pp. 108-120, June 2014.

[6] G. Palumbo and D. Pappalardo, "Charge pump circuits with only capacitive loads: optimized design," in *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 53, no. 2, pp. 128-132, Feb. 2006.

[7] S. Mandal and R. Sarpeshkar, "Low-Power CMOS Rectifier Design for RFID Applications," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 54, no. 6, pp. 1177-1188, June 2007.

[8] T. Tanzawa and T. Tanaka, "A dynamic analysis of the Dickson charge pump circuit," in *IEEE Journal of Solid-State Circuits*, vol. 32, no. 8, pp. 1231-1240, Aug. 1997.

[9] K. Kotani and T. Ito, "High efficiency CMOS rectifier circuits for UHF RFIDs using Vth cancellation techniques," *2009 IEEE 8th International Conference on ASIC*, Changsha, China, 2009, pp. 549-552.

[10] M. Stoopman, S. Keyrouz, H. J. Visser, K. Philips and W. A. Serdijn, "Co-Design of a CMOS Rectifier and Small Loop Antenna for Highly Sensitive RF Energy Harvesters," in *IEEE Journal of Solid-State Circuits*, vol. 49, no. 3, pp. 622-634, March 2014.