Low-Quiescent and Reduced-Power Zero-Current Detector for a DC-DC Switched-Mode Converter implemented in 22nm FDSOI

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***Abstract*—This paper introduces a low-quiescent and reduced-power zero current detector (ZCD) designed specifically for a DC-DC switched-mode converter operating in discontinuous current mode. The ZCD incorporates control switches strategically placed to minimize power consumption and leakage current. The ZCD operation is enabled through a ZCD controller circuit, which efficiently manages the power consumption. The controller circuit generates a voltage to control the ZCD, ensuring that the control switches are triggered only when the inductor current is about to change polarity, typically occurring when the low-side power switch of the converter is active. Once the zero current is detected, the ZCD becomes inactive after a slight delay of 1ns, as defined in this paper. The ZCD controller circuit comprises flip-flops and logic gates, managing the ZCD's activation and deactivation. Control switches are strategically placed at each branch of the ZCD circuit to optimize its efficiency. To monitor the inductor current of the DC-DC converter, the voltage polarity at one end (input side) of the inductor is sensed in relation to the ground. The ZCD is configured with transistors in reverse back gate biasing, further enhancing its performance and efficiency. The simulation results showcase impressive outcomes, with the ZCD exhibiting a quiescent current of 1.13nA and an average current of 323nA at a 0.8V supply voltage. This design is implemented using the advanced 22nm FDSOI technology, showcasing its practicality and relevance in modern circuit design.**

Keywords—zero current detector, comparator, low quiescent, low current, ZCD controller

I. INTRODUCTION

The rapid advancement of the Internet of Things (IoT) and wireless sensor networks (WSN) continues to drive innovation across various applications [1]–[5], introducing new dimensions for system enhancement. In small-form factor sensor nodes for IoT and WSN, circuit designs are meticulously tailored to achieve micro-watt level power performance [6]. Due to the limitations of energy-storing devices and stochastic energy sources, components in sensor nodes prioritize power conservation, precisely timing the delivery of energy to subsystems [7]. To maximize efficiency, an optimized power management unit (PMU) is essential. Subcircuits operating in the background can significantly influence power usage, especially during the idle mode of sensor nodes [8]. Power management integrated circuits (PMICs) play a vital role in extending the usage lifespan of IoT and sensor nodes. A typical PMIC incorporates an inductive switch-mode power supply (SMPS) device, featuring a single inductor connected to power switches, delivering output to the load side, or a supercapacitor. The current trend in PMIC architecture is the adoption of battery-less operations [7], [9], [10], which necessitate leveraging well-exploited energy sources to sustain load operation effectively. As a result, achieving improved power conversion efficiency across a wide range of load conditions becomes paramount in the design [11]. In SMPS, operation at heavy load currents involves continuous-conduction mode (CCM). However, for designs incorporating switch-mode power supplies and multiple output loads, a smaller inductor is preferred to minimize the overall device size, leading to intentional operation in discontinuous-conduction mode (DCM), particularly under light load current situations. At DCM, power conversion efficiency is diminished due to reverse current flow in the inductor [12]. If the transistor switch remains active, power losses occur due to body diode conduction, significantly impacting efficiency [13]. To mitigate the adverse effects of reverse current on power efficiency, a zero current detector (ZCD) is employed to accurately detect the zero crossing of the inductor current.

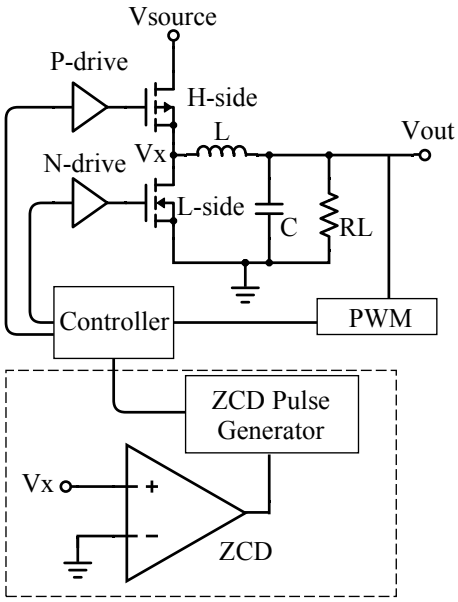
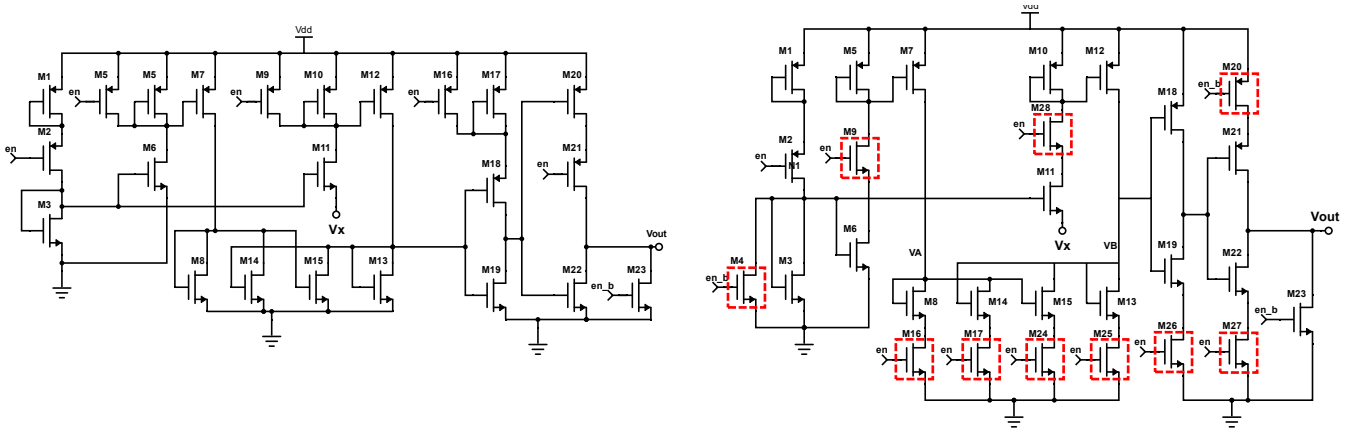


Fig. 1. DC-DC Buck Converter with ZCD

Figure 1 illustrates a ZCD integrated with a conventional DC-DC buck converter. The ZCD primarily consists of a high-speed comparator circuit, where the input node connects to one end, Vx, of the inductor, referenced to the ground [11]. During the discharging phase of the inductor, when the low-side switch is active, the voltage Vx experiences a slight increase from the negative value. Upon crossing the zero



(a) (b)

Fig. 2(a). Conventional ZCD; (b). Proposed ZCD

voltage in Vx, the comparator circuit transitions from "0" to "1". Subsequently, the flip-flop and logic gates generate the corresponding signal, which is then fed to the power switch driver to turn off the low-side switch, preventing negative current flow through the inductor. The ZCD is meticulously designed to achieve precise zero-current detection in real-time. However, this requirement for real-time detection leads to increased power consumption in the ZCD due to its fast switching and conduction characteristics. Notably, the ZCD typically accounts for 23% of the total power consumption in light load conditions, as reported in [14].

Several innovative approaches have been explored in the field of ZCD design to enhance its efficiency and accuracy. In [15], an adaptive zero-current sensing circuit is introduced, utilizing cascaded digital gates to control the ZCD's duty operation. However, the continuous operation of cascaded digital gates leads to constant energy consumption. Another study, [16], presents a fast zero current crossing detector, capable of sensing inductor current crossing the zero point during the MOS conduction phase. While effective, this implies that the ZCD remains active even during inductor peak current. In contrast, [17] proposes a high-resolution ZCD that achieves efficiency through fine and coarse digital steps. However, the usage of digital gates for high resolution significantly increases power consumption. In the work of [18], a zero-crossing point detection method is applied to a boundary current mode Power Factor Correction (PFC) converter. This study reduces the delay time in zero-crossing detection, enhancing accuracy for the boost converter under boundary current mode operation. Similarly, [19] introduces a ZCD design with an autocalibration scheme using the L-side gate signal and a shift register for precise zero current detection. Lastly, [20] presents a load-dependent ZCD, aiming to improve converter output response during light and heavy load transitions.

While the studies mentioned above showcased effective ZCD architectures, they missed incorporating a mechanism to further reduce the ZCD's power consumption. In response, this paper introduces a novel high-speed ZCD with a low quiescent current and a controller that efficiently reduces the ZCD's operating time, resulting in significant power savings.

The proposed study presents a ZCD unit with reduced power consumption and a low quiescent current. The ZCD is integrated with a control circuit and applied in a DC-DC switched-mode converter. The control circuit plays a crucial role in precisely timing the activation and deactivation of the ZCD during negative current phases. To achieve fast response times, the control circuit employs digital gates as its primary components. Through the ZCD control circuit, a control voltage is provided, effectively reducing power consumption, minimizing switching loss, and lowering conduction loss associated with the ZCD's operation. This innovative approach aims to enhance the overall efficiency of the ZCD and the DC-DC converter.

II. Operation Principle and Proposed ZCD Circuit

A. ZCD Design

Figure 2(a) illustrates the conventional ZCD circuit, which consists of an input differential pair, a cross-coupled current mirror, a common gate pre-amplifier, a biasing circuit, and a buffer circuit [14]. Initially, the voltage Vx is amplified through the common gate pre-amplifier to enhance the resolution in detecting Vx's zero point. This pre-amplifier also ensures isolation between the differential pair's input and the power switches, effectively minimizing switching noise. Transistor M11's source terminal serves as the input node for the Vx signal, while transistor M10 acts as the diode-connected load, contributing to a low input impedance when the Ron of transistor M10 is small, making it an effective current buffer for ZCD applications. To establish the necessary biases for transistors M6 and M11, their gate terminals are connected to the biasing circuit, which comprises transistors M1 and M3. This biasing circuit is responsible for providing the appropriate biases to ensure

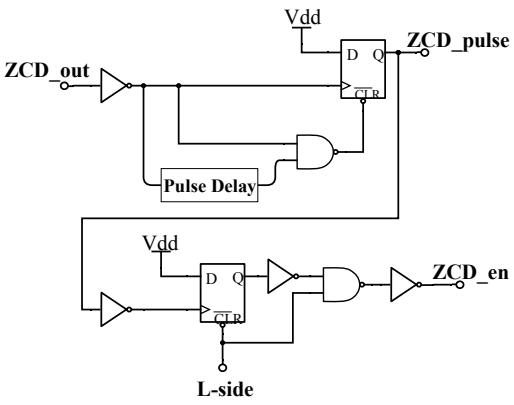


Fig. 3. ZCD Control Unit

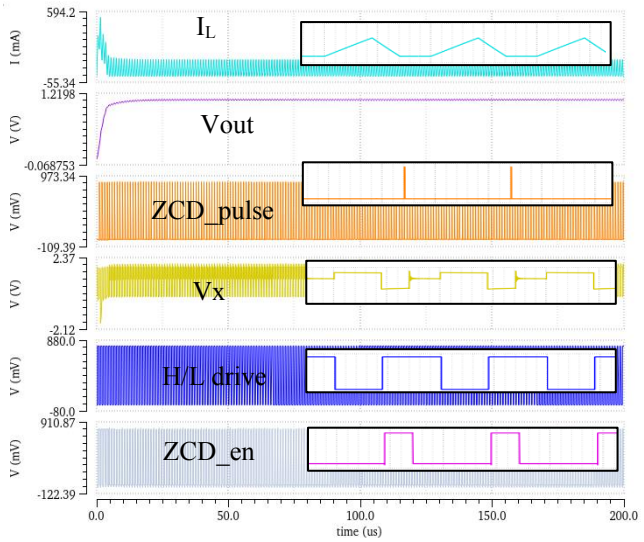


Fig. 4. ZCD Transient Response

proper operation of transistors M6 and M11 in the ZCD circuit.

The cross-coupled current mirror in the ZCD circuit is configured as positive feedback, which plays a crucial role in the decision-making process or comparison of inputs. As shown in the figure, one input comes from the Vx voltage and is compared to a reference voltage of 0V, which is connected to the source terminal of transistor M6. Since the source terminal of transistor M6 is fixed to ground, a constant bias voltage is applied to the gate terminal of transistor M7, ensuring that M7 carries a constant drain current to one side of the cross-coupled current mirror (M8, M14). On the other hand, transistor M12 has its gate terminal connected to the drain terminal of M10, receiving a varying bias voltage due to the input voltage at the source terminal of M11. Consequently, M12 supplies drain current to the other side of the cross-coupled current mirror (M13, M15).

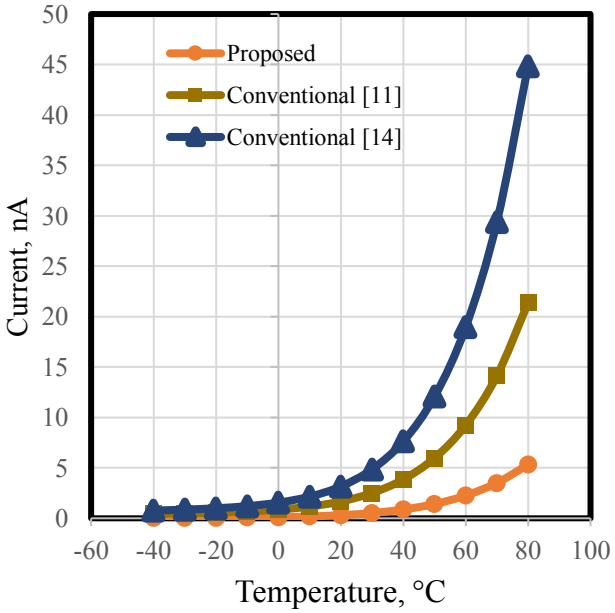


Fig. 5. Quiescent Current vs Temp Plot of Conventional and Proposed ZCD

As the input voltage Vx increases, the drain current in M12 decreases, leading to a reduction in the gate bias for transistors M13 and M14, thereby affecting their drain currents. In contrast, the drain current in M7 remains constant, providing a positive bias for transistors M8 and M15. Consequently, M8 and M15 experience higher currents, which, in turn, provide feedback to the gate bias of M3 and M14, further reducing their drain currents. The drain of M13 is connected to the buffer circuit to achieve rail-to-rail output voltage.

The positive feedback of the cross-coupled current mirror produces hysteresis. The expression is described by the formula [21]:

$$H_{ysteresis} = P'I_{M6} - PI_{M6} \tag{1}$$

Where P is the ratio of the current of M12 to M7 and P' is the reverse current, can be given by,

$$P = \frac{(V_B - V_{tn})^2 + \frac{K_{M14}}{K_{M13}}(2V_A - 2V_{tn} - V_B)\,V_B}{(V_A - V_{tn})^2 + \frac{K_{M14}}{K_{M13}}(V_B - V_{tn})^2} \tag{2}$$

$$P' = \frac{(V_B - V_{tn})^2 + \frac{K_{M14}}{K_{M13}}(V_A - V_{tn})^2}{(V_A - V_{tn})^2 + \frac{K_{M14}}{K_{M13}}(2V_B - 2V_{tn} - V_A)\,V_A} \tag{3}$$

$(V_A\text{-}V_{tn})^2$ is derived from the large and small analysis given by,

$$(V_B - V_{tn})^2 = \frac{K_{M13}\,K_{M12}}{K_{M10}\,(K_{M13}^2 - K_{M14}^2)}\left(I_{M11} - I_{M6} + \frac{K_{M9}}{K_{M13}}I_7 - I_{12}\right) \tag{4}$$

$$(V_A - V_{tn})^2 = \frac{K_{M14}\,K_{M12}}{K_{M10}\,(K_{M13}^2 - K_{M14}^2)}\left(I_{M11} - I_{M6} + \frac{K_{M13}}{K_{M14}}I_7 - I_{12}\right) \tag{5}$$

The control of hysteresis current relies on the current at M5, which remains constant since M6 has a ground-connected source. In a different scenario, if the ratio of K_{M14}/K_{M13} is approximately set to 1, meaning $K_{M14} \approx K_{M13}$, it is observed that $(V_A\text{-}V_{tn})^2$ and $(V_B\text{-}V_{tn})^2$ become nearly zero. As a result, the hysteresis current approaches zero. This condition transforms the circuit into a comparator without hysteresis.

B. Proposed ZCD Design

In Fig. 2(b), multiple enable transistors are strategically placed in each branch of the circuit to control the ZCD's operation mode (enable, disable). These enable transistors also play a crucial role in minimizing leakage current during the ZCD's inactivity. Their arrangement has minimal impact on the ZCD's performance, as they operate discretely in either the cut-off or saturation region. Transistor M2 is positioned between M1 and M3, enabling it to disconnect node N1 from VDD during the disabled mode. Transistor M4 biases the gates of transistors M3, M6, and M11 to the ground source, causing them to operate in the cut-off region when their gates are grounded. Transistors M9 and M28 ensure that the gate terminals of M7 and M12 are disconnected, preventing their operation in the saturation region. Similarly, transistors M16,

M17, M24, and M25 prevent any current flow in their corresponding branches when their gate terminals receive zero voltage. Transistor M26 disconnects its branch from the ground to prevent current flow, while M20 disconnects M21 from VDD and M27 disconnects M22 from the ground. Lastly, M23 pulls down the Vout node to ground during the disabled mode to ensure it stays at zero voltage.

C. *Proposed ZCD Control Unit*

The control unit, illustrated in Fig. 3, plays a vital role in the ZCD circuit's operation. It generates two key outputs: ZCD_pulse and ZCD_en. ZCD_pulse is a 1ns pulse that indicates the detection of the inductor's zero current. This pulse is generated based on the ZCD's output and is utilized to produce the control voltage ZCD_en through flip-flops and digital gates. The DC-DC converter employs ZCD_en as a control voltage for the L-side switch, effectively preventing the flow of negative current through the inductor. Additionally, ZCD_en serves as the control voltage for the enable transistors in the ZCD. To generate the pulse, a flip-flop and pulse delay mechanism are utilized, with the ZCD block's output acting as the input. The rising edge of the pulse aligns with the rising edge of the ZCD output, while the pulse delay resets the flip-flop after the 1ns delay, causing the falling edge of ZCD_pulse. The resulting ZCD_en signal efficiently controls the enable transistors, mitigating unnecessary on-time of the ZCD. For this purpose, a combination of flip-flops and digital gates processes the input signals ZCD_pulse and L-side clock.

III. Simulation and Results

The proposed ZCD circuit design is implemented using Global Foundry's advanced 22nm FDSOI technology. The pre-layout of the ZCD block occupies a compact area of 160 sq um. This cutting-edge FDSOI technology offers significant advantages in terms of power consumption compared to traditional partially-depleted SOI technology [22]–[24].

In the simulation, the DC-DC buck converter model operates at a 1MHz switching frequency with a 2uH inductor and 1uF capacitor, utilizing the discontinuous-conduction mode (DCM). The load range spans from 2mA to 40mA, providing an output voltage of 0.8-1.1V. Remarkably, the ZCD can handle input signal frequencies of up to 40MHz, making it suitable for applications with multiple input-source DC-DC converters featuring dynamic switching frequencies.

In Fig. 4, we observe the inductor current, control voltages, and ZCD pulse generated from the Vx node of the DC-DC converter. The ZCD circuit is intelligently enabled at the start of the inductor's discharging phase or during the "on" time of the L-side power switch. As soon as the inductor current crosses the zero axis, the ZCD pulse, with a precise 1ns pulse width, is generated. Simultaneously, the ZCD_en signal turns "LOW," efficiently disabling the ZCD operation.

The ZCD pulse exhibits an impressively low delay of less than 1ns. Although some practical delay is present, it is negligible, lasting for a very short period of less than 1ns. This remarkable performance significantly reduces the impact of reverse current in the system.

The ZCD's performance is further analyzed across a range of temperatures and process corners to ensure its robustness and efficiency. To ensure a fair comparison, the conventional ZCD is simulated in the same technology node as the proposed design. The quiescent currents are compared under different process corners, namely SS, SF, TT, FS, and FF, representing slow, typical, and fast variations.

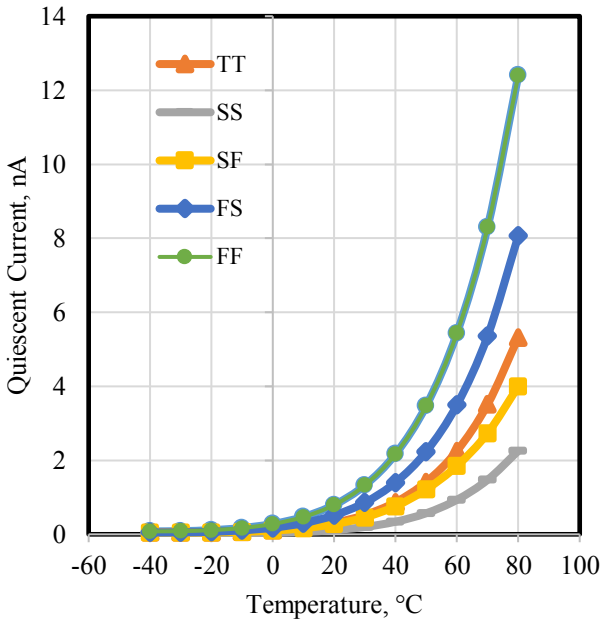


Fig. 6. Corner Simulation of the Proposed ZCD

Fig. 5 displays the quiescent current of both the conventional and proposed ZCD designs over the temperature range of -40 to 80 degrees Celsius. Remarkably, the proposed ZCD exhibits the lowest leakage current when compared to the conventional design. The average leakage current of the conventional ZCD was found to be 4.84nA and 9.88nA.

Furthermore, Fig. 6 showcases the quiescent current of the ZCD at different process corners. Although the variability among the corners increases with temperature, the average leakage current of the proposed ZCD remains impressively lower than the conventional design, which itself is already

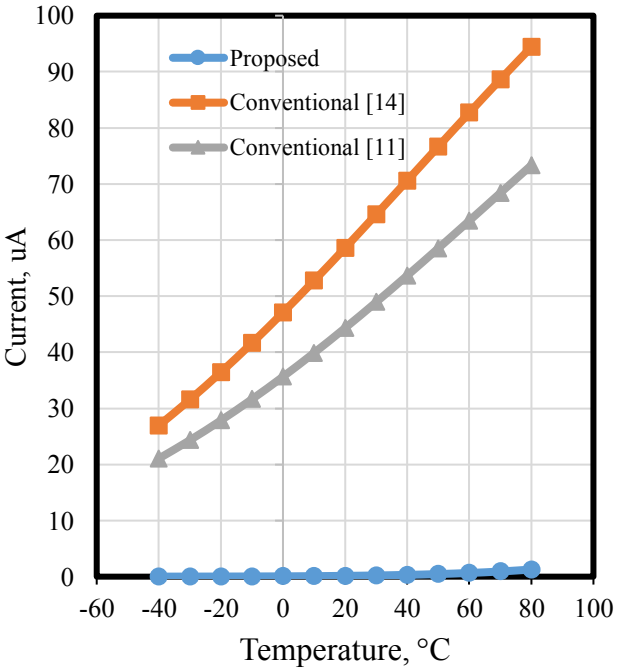


Fig. 7. Current Consumption of Conventional and Proposed ZCD

TABLE 1. COMPARISON TO THE PRIOR WORKS

Parameter	Vratislav Michal [16]	Mohammad Alhawari [17]	Young-Jun Park [15]	Xianzhi Meng [13]	Sally Safwat Amin [14]	This study
Input voltage	2.5-4.8V	0.6V, 1.2V	2.2-3.3V	2.5-4V	0.1-1V	0.3-1.8V
Technology	0.13um	65nm	0.13um	-	28nm FDSOI	22nm FDSOI
Output voltage	-	1.35V	1.7V	5V	0.4-1.4V	0.8V
Load range	6.1-11mA	-	0.01-20mA	<1A	-	5-40mA
Frequency f_{SW}	3.2MHz	17kHz	2.5MHz	1MHz	500kHz	1MHz
Inductor	1uH	47uH	3uH	1uH	10uH	1uH
Capacitor	-	50nF	3uF	-	1uF	2uF
Average Current	-	~400uA	-	-	2.23uA	323nA
Quiescent Current	15uA @3.6V	-	-	4uA	262nA @ 1V	1.13nA
Operation	CCM/DCM	CCM/DCM	DCM	DCM	CCM/DCM	DCM

small. In the typical corner, the average quiescent current of the proposed ZCD measures 1.13nA, demonstrating an outstanding 85% reduction compared to the conventional ZCD.

Fig. 7 illustrates the average current consumption of the DC-DC converter operating in DCM mode across a temperature range from -40 to 80 degrees Celsius. In the case of the conventional ZCD control setup, the current consumption varies from 20uA to 75uA when using a ZCD as presented in [14], and 25uA to 95uA when utilizing a typical ZCD comparator. However, with the proposed ZCD combined with the control components, the current consumption exhibits an impressive range of 0.007uA to 1.27uA.

In the nominal corner, the measured average current consumption is 323nA for the ZCD and 0.2uA for the control circuit. This remarkable result translates to a significant 90% reduction in current consumption without compromising the ZCD's performance.

Table 1 presents a comprehensive comparison between the proposed ZCD and previous works for the DC-DC converter in DCM mode, with a specific focus on current consumption and quiescent current. The table highlights the specifications and performance metrics, emphasizing the distinctions among the designs. Significantly, the proposed ZCD excels in delivering lower quiescent current during idle mode compared to its predecessors. Moreover, the current consumption of the proposed ZCD stands out remarkably, showcasing a substantial reduction when compared to existing designs, solidifying its position as an efficient and superior solution.

IV. CONCLUSION

This paper presents a novel low-quiescent and reduced-power zero current detector (ZCD) designed for DC-DC switched-mode converters operating in discontinuous current mode. The proposed ZCD includes strategically arranged control switches on each branch to effectively minimize leakage current. Furthermore, a controller circuit is integrated into the ZCD design, significantly reducing power consumption by generating the control voltage that enables efficient ZCD operation.

The effectiveness of the proposed ZCD is demonstrated in a 1uH single inductor DC-DC buck converter operating in DCM with a 1MHz switching frequency. Measurement results reveal an impressively low quiescent current of 1.13nA, showcasing an 85% reduction compared to prior works. Additionally, the average current consumption of the combined ZCD and control unit is merely 323nA at a 0.8V supply, indicating a remarkable 90% reduction in current consumption. These results highlight the significant advancements achieved with the proposed ZCD, making it a promising candidate for energy-efficient and high-performance DC-DC converter applications.

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REFERENCES

[1] A. Iji, X. Zhu, and M. Heimlich, "High gain/power quotient variable-gain wideband low-noise amplifier for capsule endoscopy application," *Microwave and Optical Technology Letters*, vol. 54, Nov. 2012, doi: 10.1002/mop.27111.

[2] A. Iji, X. Zhu, and M. Heimlich, "A 4.5 mW 3–5 GHz low-noise amplifier in 0.25-µm silicon-on-insulator CMOS process for power-constraint application," *Microwave and Optical Technology Letters*, vol. 55, Jan. 2013, doi: 10.1002/mop.27262.

[3] X. He, X. Zhu, L. Duan, Y. Sun, and C. Ma, "A 14-mW PLL-Less Receiver in 0.18- \mu\hboxm CMOS for Chinese Electronic Toll Collection Standard," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 61, no. 10, pp. 763–767, Oct. 2014, doi: 10.1109/TCSII.2014.2345303.

[4] J. A. Hora, X. Zhu, and E. Dutkiewicz, "Simplified Over-Temperature Protection Circuit Structure for WSN/IoT Device Power Management," in *2019 13th International Conference on Sensing Technology (ICST)*, Dec. 2019, pp. 1–4. doi: 10.1109/ICST46873.2019.9047726.

[5] J. A. Hora, M. A. Mayormita, J. R. C. Rebollos, X. Zhu, and E. Dutkiewicz, "On-Chip Inductor-Less Indoor Light Energy Harvester with Improved Efficiency for WSN/IoT Device Design," in *2019 13th International Conference on Sensing Technology (ICST)*, Dec. 2019, pp. 1–6. doi: 10.1109/ICST46873.2019.9047728.

[6] V. Pecunia, L. G. Occhipinti, and R. L. Z. Hoye, "Emerging indoor photovoltaic technologies for sustainable internet of things," *Advanced Energy Materials*, vol. 11, no. 29, p. 2100698, Aug. 2021, doi: 10.1002/aenm.202100698.

[7] K. K. C. Adrivan and J. A. Hora, "A Nano-Watt, Subthreshold Self-Biased CMOS Voltage Reference without Resistors and BJT," in *TENCON 2022 - 2022 IEEE Region 10 Conference (TENCON)*, Nov. 2022, pp. 1–5. doi: 10.1109/TENCON55691.2022.9977986.

[8] J. A. Hora, A. C. Arellano, X. Zhu, and E. Dutkiewicz, "Design of Buck Converter with Dead-time Control and Automatic Power-Down System for WSN Application," in *2019 IEEE Wireless Power Transfer Conference (WPTC)*, Jun. 2019, pp. 582–586. doi: 10.1109/WPTC45513.2019.9055685.

[9] Y.-H. Lee *et al.*, "Minimized transient and steady-state cross regulation in 55nm CMOS single-inductor dual-output (SIDO) step-down DC-DC converter," in *2010 IEEE Asian Solid-State Circuits Conference*, Nov. 2010, pp. 1–4. doi: 10.1109/ASSCC.2010.5716558.

[10] M. E. C. Andam, J. M. B. Quinalayo, and J. A. Hora, "Reconfigurable Dual-band Radio Frequency Energy Harvester utilizing 900MHz and 2.4GHz Frequency Band," in *TENCON 2022 - 2022 IEEE Region 10 Conference (TENCON)*, Nov. 2022, pp. 1–6. doi: 10.1109/TENCON55691.2022.9977669.

[11] Y. Gao, S. Wang, H. Li, L. Chen, S. Fan, and L. Geng, "A novel zero-current-detector for DCM operation in synchronous converter," in *2012 IEEE International Symposium on Industrial Electronics*, May 2012, pp. 99–104. doi: 10.1109/ISIE.2012.6237066.

[12] R. C. M. Calam, J. A. Hora, O. J. L. Gerasta, X. Zhu, and E. Dutkiewicz, "A Self-Calibrating Off-Time Controller for WSN/IoT Synchronous Non-Inverting Buck-Boost DC-to-DC Converter Application," in *2019 IEEE International Circuits and Systems Symposium (ICSyS)*, Sep. 2019, pp. 1–4. doi: 10.1109/ICSyS47076.2019.8982410.

[13] X. Meng, K. Sun, J. Xi, and L. He, "Real time zero current detection with low quiescent current for synchronous DC-DC converter," in *2017 IEEE 26th International Symposium on Industrial Electronics (ISIE)*, Edinburgh, United Kingdom: IEEE, Jun. 2017, pp. 839–843. doi: 10.1109/ISIE.2017.8001355.

[14] S. S. Amin and P. P. Mercier, "Misimo: a multi-input single-inductor multi-output energy harvesting platform in 28-nm fdsoi for powering net-zero-energy systems," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 12, pp. 3407–3419, Dec. 2018, doi: 10.1109/JSSC.2018.2865467.

[15] Y.-J. Park *et al.*, "A design of a 92. 4% efficiency triple mode control dc–dc buck converter with low power retention mode and adaptive zero current detector for iot/wearable applications," *IEEE Transactions on Power Electronics*, vol. 32, no. 9, pp. 6946–6960, Sep. 2017, doi: 10.1109/TPEL.2016.2623812.

[16] V. Michal and D. Chesneau, "Time domain CCM/DCM boundary detector with zero static power consumption for integrated high-efficiency step-down DC/DC converters," in *2016 International Conference on Applied Electronics (AE)*, Pilsen, Czech Republic: IEEE, Sep. 2016, pp. 183–186. doi: 10.1109/AE.2016.7577269.

[17] M. Alhawari, B. Mohammad, H. Saleh, and M. Ismail, "An all-digital, CMOS zero current switching circuit for thermal energy harvesting," in *2015 European Conference on Circuit Theory and Design (ECCTD)*, Trondheim, Norway: IEEE, Aug. 2015, pp. 1–4. doi: 10.1109/ECCTD.2015.7300094.

[18] Jizhe Wang, K. Yoshimura, and F. Kurokawa, "Zero-crossing point detection using differentiation circuit for boundary current mode PFC converter," in *2015 IEEE 2nd International Future Energy Electronics Conference (IFEEC)*, Taipei, Taiwan: IEEE, Nov. 2015, pp. 1–6. doi: 10.1109/IFEEC.2015.7361510.

[19] J. Baek, H.-M. Lee, and S.-U. Shin, "Triple-mode switched-inductor-capacitor dc-dc buck converter with reusable flying capacitor and bang-bang zero-current detector for wide load current range," *Electronics*, vol. 9, no. 8, p. 1202, Jul. 2020, doi: 10.3390/electronics9081202.

[20] C.-L. Chen, W.-J. Lai, T.-H. Liu, and K.-H. Chen, "Zero current detection technique for fast transient response in buck DC-DC converters," in *2008 IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2008, pp. 2214–2217. doi: 10.1109/ISCAS.2008.4541892.

[21] N. K. Chasta, "High Speed, Low Power Current Comparators with Hysteresis," *International Journal of VLSI Design & Communication Systems*, vol. 3, no. 1, pp. 85–96, Feb. 2012, doi: 10.5121/vlsic.2012.3107.

[22] A. Iji, X. Zhu, and M. Heimlich, "A folded-switching mixer in SOI CMOS technology," in *2012 IEEE 55th International Midwest Symposium on Circuits and Systems (MWSCAS)*, Aug. 2012, pp. 458–461. doi: 10.1109/MWSCAS.2012.6292056.

[23] A. Iji, X. Zhu, and M. Heimlich, "Low power, high gain, low noise amplifier (LNA) for ultra wide-band applications," *Microwave and Optical Technology Letters*, vol. 55, Jun. 2013, doi: 10.1002/mop.27588.

[24] A. Iji, X. Zhu, M. Heimlich, and Y. Sun, "An OTA-C filter in SOI CMOS for UWB application," in *2012 IEEE 55th International Midwest Symposium on Circuits and Systems (MWSCAS)*, Aug. 2012, pp. 93–96. doi: 10.1109/MWSCAS.2012.6291965.