Low Power Gate Voltage Controlled Schmitt Trigger with Adjustable Hysteresis and $0.1V_{th}$ Margin in 22nm FDSOI

Marc Macbeth M. Toledo[1] and Jefferson A. Hora[2]
Microelectronics laboratory, Department of Electrical Engineering and Technology
Mindanao State University - Iligan Institute of Technology
Iligan City, Philippines 9200
marcmacbeth.toledo@g.msuiit.edu.ph[1] jefferson.hora@g.msuiit.edu.ph[2]

***Abstract*—This paper introduces a Schmitt trigger with adjustable hysteresis, specifically developed for low power performance and fabricated using 22nm FDSOI technology. The proposed design incorporates a dynamic threshold voltage generation technique to achieve both reduced power consumption and high noise immunity. The voltage-controlled hysteresis is adjustable to enable the design to be customized for different applications. The Schmitt trigger is implemented using a standard CMOS process and the circuit performance is analyzed using Cadence Virtuoso simulation. The outcome presents that the suggested design achieves a low power consumption ranging from nW to pW and a high noise immunity with an adjustable hysteresis of 0 V to 0.4V to both gate voltages. The suggested design is well-suited for low power requirements in various digital circuit applications, including memory, microprocessors, and sensors.**

***Index Terms*—Low Power; Dynamic Threshold Voltage; V ltage Controlled Schmitt Trigger; Adjustable Hysteresis; 22nm FDSOI; Noise Immunity; CMOS; Digital Circuits.**

I. Introduction

Technology has become an essential part of our lives since the global pandemic began. We now rely on online meetings, virtual conferences, and remote classes conducted wirelessly from our homes. As a result, devices such as laptops, smartphones, and tablets, which are crucial for these activities, require longer battery life. In response to this requirement, designers of mobile integrated circuits (ICs) have directed their efforts towards decreasing power consumption by scaling down the supply voltage. This has led to the development of sub-threshold circuits and a significant decrease in the supply voltage.Nevertheless, the reduction in supply voltage has an adverse effect on the circuit's ability to withstand noise, thereby compromising its noise immunity.

The Schmitt trigger (ST) holds great significance as a fundamental component in electronic communication systems, playing essential roles in communication, measurement, and signal processing. ST's are vital for smart devices and IoT, enabling their full functionality. They are extensively utilized in analog and digital circuits due to their capability to convert fluctuating voltages into stable logical signals (ones or zeros).

ST enhances a circuit's noise immunity by utilizing hysteresis, which adjusts the switching threshold based on the input signal transition. This ensures that the output remains unaffected by small input variations and provides protection against unwanted electromagnetic noise [1]- [5].

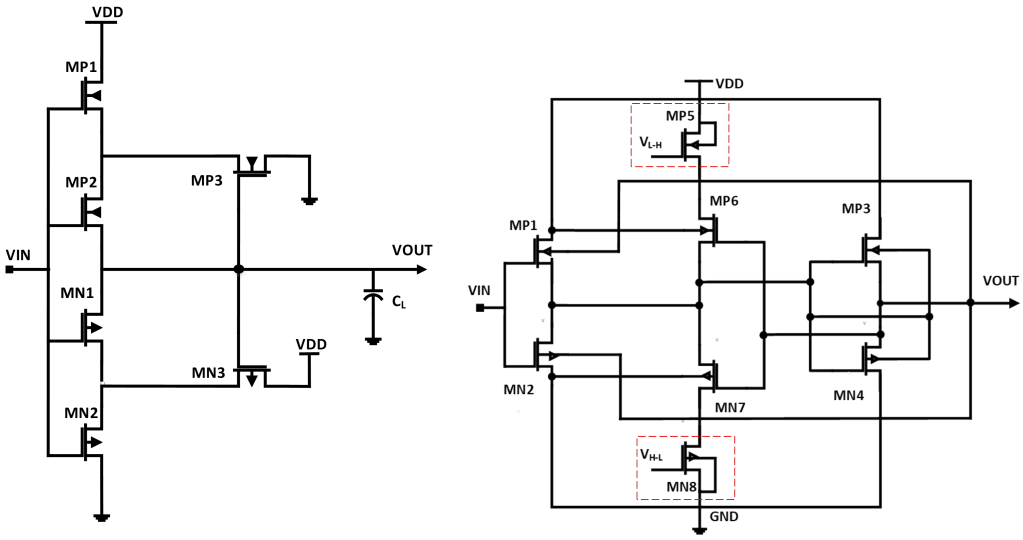
This paper describes a Dynamic Threshold - MOS (DTMOS) technology that has been widely applied in various integrated circuit designs, especially in low-power and high-speed applications. By dynamically adjusting the threshold voltage, DTMOS devices can achieve improved performance in terms of speed, power consumption, noise immunity, and other desirable characteristics for specific circuit requirements for low power application including SRAMs [6]. To boost voltage gain and enhance performance, an OTA can be added to an ST circuit [7]. Unlike the old-fashioned partially-depleted SOI, the FDSOI technology provides superior performance in terms of power consumption [1]- [5]. The circuit design being proposed makes use of a 22nm Fully Depleted Silicon-On-Insulator (FDSOI) technology and was simulated using Cadence Virtuoso.

II. Circuit Description

A. Development of Schmitt Trigger

As time passes, the development of Schmitt Triggers becomes common, and one advantage for circuit designers is to develop unique techniques and architectures to claim the novelty of their study. In this paper, one of the main novelties is the replacement of an alternative architecture in an energy harvesting circuit that uses a hysteresis comparator. According to [4], the main difference between Schmitt triggers and comparators is primarily evident in their DC transfer characteristics.In contrast to comparators that possess a single switching threshold, Schmitt triggers exhibit multiple switching thresholds for both positive and negative input signals, a characteristic referred to as hysteresis. This hysteresis allows the Schmitt trigger to resist unwanted noise, as it remains unresponsive if the input signal's noise level is below the switching threshold difference.

Another novelty introduced is in terms of the architecture. Prior studies have designed adjustable hysteresis Schmitt triggers using body bias to adjust their hysteresis [8], [9], [11], [12]. However, body biasing is considered risky due to leakage current, particularly in low-power applications [8]. The core focus of this paper is reducing power consumption, noise figure, and leakage current. Instead of using body biasing to control the hysteresis of the ST, this paper proposes the use of a gate-voltage controlled MOS for hysteresis



(a) Conventional (b) Proposed

Fig. 1. Schmitt Triggers

adjustment. This approach effectively reduces the leakage current caused by body biasing.

B. Conventional Schmitt

A well-known conventional CMOS Schmitt trigger circuit is presented by [13] in Fig. 1(a) However, no in-depth research has ever been done on the circuit's architecture. It is just defined in a simple manner that the transition is fast [14]. The hysteresis were also fixed in which there is a limited functionality on the presented design of [13].

C. Prior Study

Different types of Schmitt triggers were researched, including those designed by [18], [19], [20], and [21]. These designs varied in their implementation, with [18] utilizing a two-stack MOS transistor, [19] developing a logical threshold ST controlled by voltage, reference [20] proposing a schmitt based on the work of [18], reference [11] utilized a body biasing to reach various switching thresholds for zero to one and one to zero logic, and [21] employing a design with two static inverters and distinctive threshold voltages.

One common flaw in these works is that hysteresis is influenced by device size, supply voltages, and process parameters. To address this, [10] introduced novel methods that modify the circuit architecture, incorporating feedback from the output to the internal circuit nodes.

Researchers built upon the conventional schmitt trigger presented in [13] for their innovations. [18] reimagined the conventional design, while [12] enhanced [18]'s work by introducing body biasing to adjust the hysteresis. [8] further improved upon [12]'s study, combining techniques from [11]. Additionally, [9] utilized [8]'s design and incorporated a DTMOS on the first stage inverter of the ST. Furthermore, [9] designed a Schmitt Trigger AND gate and a Schmitt trigger OR gate.

III. Proposed ST Architecture

In order for us to prevent the enumerated drawback by [27], recent STs will be modified in the hysteresis adjustment part. Instead of [8], [9], [11], and [12]'s Variable Threshold CMOS (VTCMOS) in controlling the hysteresis of a Schmitt trigger, this paper will replace the hysteresis adjustment with a cascoded CMOS using gate biasing to control the hysteresis of an ST.

"Fig. 1(b)." Illustrates the suggested structure of the study. Previous techniques which is the DTMOS on the first stage and second stage inverters will be retained while the Voltage that controls the hysteresis adjustment will be replace a cascoded PMOS (MP5 and MP6) and a cascoded NMOS (MN7 and MN8). Since gate biasing is one of the conventional biasing techniques, this will ease the struggle in terms of the drawbacks of the Body-biasing. This circuit shown will still be applicable in low power application since DTMOS technique is being applied.

According to [9], it is necessary to decrease the DTMOS threshold voltage below the supply voltage to ensure that the transistor operates in the saturation region. This precaution is taken due to the supply voltage's proximity to the standard threshold voltage value of 0.4V. By establishing a connection between the gate and substrate, a forward body bias condition is achieved at the body-to-source junction, resulting in a reduction in the threshold voltage. By employing a negative source-to-body bias configuration, this approach leverages the body effect to effectively decrease the threshold voltage. The first-stage inverter's substrate bias, depicted in the above Fig. 1(b), is coupled to VOUT and unaffected by the node receiving input signals. As a result, the first stage's threshold voltage fluctuates depending on the value of VOUT, and this architecture is known as variable threshold voltage CMOS (VTCMOS).The activation voltage of each transistor is higher in the scenario illustrated in Fig. 1(b) compared to typical DTMOS. This is due to the zero-body bias condition set for the output transition in each transistor of the initial stage. The following equations presented in [1] offer a means to define the switching threshold voltage.

$$V_{H-L} = \frac{V_{DD} \ + \ \gamma \text{ x } V_{t,N} \ - \ |V_{t_0,P}|}{\gamma \ + \ 1} \tag{1}$$

$$V_{L-H} = \frac{V_{DD} \ - \ |V_{t,P}| \ + \ \gamma \text{ x } V_{t_0,N}}{\gamma \ + \ 1} \tag{2}$$

where $V_{t,N(P)}$ is the value for the threshold voltage of the N-MOS(P-MOS) for the Forward Bias condition. $V_{t0,N(P)}$ is the threshold voltage of the zero-bias condition while $\gamma = \sqrt{\beta_N/\beta_P}$. β_P and β_N are the parameters of the PMOS and NMOS's transconductance respectively.

Eq. 1 is used to determine the threshold voltage from high to low or from 1 to 0 going due to MN8. While eq. 2 is used to determine the threshold voltage from low to high or from 0 to 1 going due to MP5 .

The suggested DTMOS Schmitt trigger, incorporating VTCMOS, offers a superior solution to mitigate the impact of noise and threshold voltage variation on MP1 and MN2 (as shown in Fig. 1(b)), considering the feedback body bias (VOUT). This approach improves noise immunity while employing a reduced number of transistors and lower power consumption compared to the conventional method.

The calculation of the hysteresis width can be obtained using the equation derived from equations (1) and (2) as follows:

Hysteresis Width = $V_{LH} - V_{HL}$

$$= \frac{|V_{t_0,P}| \ - \ |V_{t,P}| \ + \ \gamma \text{ x } (V_{t_0,N} - V_{t,N})}{\gamma \ + \ 1} \tag{3}$$

IV. Simulation Results

The Proposed Voltage Gate Controlled Schmitt Trigger is designed in 22nm FDSOI(Fully Depleted Siliocn On Insulator. One important advantage of the FDSOI is improving Power Efficiency: FD-SOI technology enables better power efficiency compared to traditional bulk CMOS. The fully depleted structure reduces leakage current and enhances control over the transistor, resulting in lower power consumption.

Fig. 2(a). shows the ranges of the adjusted voltage threshold from low to high $V_{t_{L-H}}$ and high to low $V_{t_{H-L}}$ than can be adjust from 0 V to 0.4 V for both gate voltage. The power dissipation is in terms of nanowatts to picowatts depending on the duration of the switching period.

Furthermore, it demonstrates the resulting output signal when a triangular waveform (0.4 Vpp, 1 MHz)is applied as the input signal.The intersection points between the input signal and output signal signify the switching threshold voltages that can be ascertained.

Fig. 2(b). and 2(c). show the switching threshold voltage V_{L-H} and V_{H-L} . The V_{L-H} can be adusted from 0.19V to 0.29V and the V_{H-L} from 0.014V to 0.16V. The margin of switching threshold voltages for V_{L-H} and V_{H-L} is 10% and 14.6% respectively.

Fig. 3. illustrates the DC voltage transfer characteristics for various V_{H-L} and V_{L-H} values.

A small hysteresis window is evident on the aforementioned figure. This window refers to the range or gap between the upper and lower thresholds at which a system or device transitions between different states in which it provides several advantages.

A. Stability

A small hysteresis window can provide better stability and reduce oscillations or rapid state changes in a system. By minimizing the gap between the upper and lower thresholds, the system is less likely to switch back and forth rapidly between states, resulting in a more stable and consistent behavior.

B. Precision

In some applications, precision is crucial. A small hysteresis window allows for more precise control and detection of specific conditions or events. By narrowing the range at which a transition occurs, the system can respond more accurately to changes in the input signal or environment.

C. Responsiveness

A small hysteresis window can enable faster response times in systems that require quick reaction or adaptation to changing conditions. With a smaller gap between thresholds, the system can detect and react to changes more rapidly, reducing any delay in the system's response.

D. Energy Efficiency

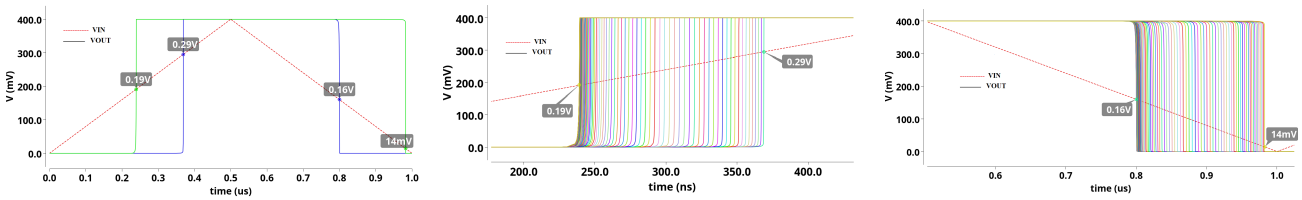
In systems where energy efficiency is a concern, a small hysteresis window can help minimize power consumption. By reducing the range of the hysteresis, the system can transition between states with less energy expenditure, as it requires less time or effort to switch from one state to another.

It is worth noting that achieving the optimal hysteresis window size is of significant importance and it depends on a specific application, system requirements, and environmental factors. In some cases, a larger hysteresis window may be preferred to account for noise or variability in the system, while in others, a small hysteresis window may be desirable for the aforementioned advantages.

Fig. 4. presents the simulation result of Monte Carlo analysis with 200 iterations using 6-sigma. Monte Carlo Analysis is employed in simulating the ST to obtain more accurate estimations, considering factors such as process variation and reliability [27]. There is a 10% tolerance from the input voltage during simulation. Samples in green are the process variation in the TT Corner while the red and blue samples are the process variation for FF and SS Corner respectively. The result shows that the circuit design can tolerate the expected variations and uncertainties without significantly deviating from the desired performance. It indicates that the design is less sensitive to variations in component values, process parameters, or environmental conditions.

V. Conclusion

A Schmitt trigger employing the dynamic threshold gate voltage controlled technique is introduced in this study. It was the circuit incorporates three-stage CMOS inverters and allows for individual adjustment of the switching thresholds. Through Monte Carlo simulations, the circuit design was thoroughly evaluated in 22nm FDSOI technology. The results demonstrated that the design does not only achieved low power consumption but also exhibited high noise immunity. The successful completion of the Monte Carlo simulations (SS, TT, and FF) [28] further validated the circuit's robustness



(a) ST Output (b) Low to High (c) High to Low

Fig. 2. Input and Output Waveforms

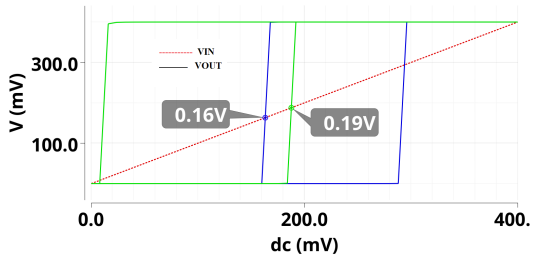


Fig. 3. DC Voltage Transfer Characteristics

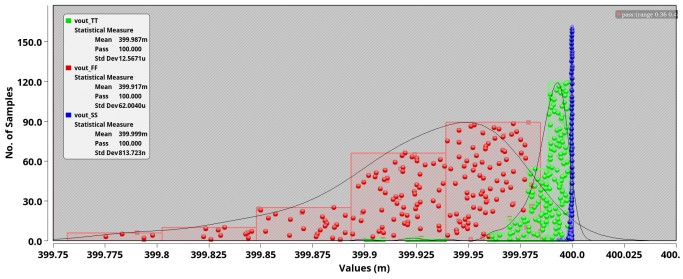


Fig. 4. Process Variation Simulation

and its ability to maintain desirable performance characteristics under various parameter variations and environmental conditions .In addition to the aforementioned attributes, the circuit simulated in 22nm FDSOI technology exhibited the advantage of a small hysteresis window. The small hysteresis window is beneficial as it allows for precise and reliable switching behavior, ensuring accurate operation and reducing the possibility of false triggering or unwanted fluctuations in the circuit. The voltages can be manipulated to independently adjust the switching threshold voltages V_{H-L} and V_{L-H}.

Table 1 shows the summary of the related studies on schmitt triggers.

This paper utilizes the smallest technology node compared to all the listed studies. The method of this study is holistic in approach since it uses some combined techniques to further improve the ST with an ease of configuration in hysteresis adjustment. Since the hysteresis of this study is also adjustable, it is an edge with the other studies for this can also be used in low power applications. This paper is also stable in terms of process variation with an extra advantage in noise immunity.

ACKNOWLEDGMENT

This paper would like to acknowledge the support provided by the Department of Science and Technology – Science Education Institute (DOST-SEI) thru the Engineering for Research and Development (ERDT) Program together with the Mindanao State University-Iligan Institute of Technology and the Institute's Microelectronics Laboratory for helping make this work possible. Progress in this work is utilized as a preliminary circuit design block for the funded project by the Department of Science and Technology (DOST), Philippines and monitored by DOST-PCIEERD for the project titled Energy Harvesting for Battery-less IoT Device Operation under the program Center for Integrated Circuits and Devices Research (CIDR). Special Thanks to XINYX DESIGN for sponsoring the procurement of Cadence IC Design Software tools for the simulation of this work.

REFERENCES

[1] A. Iji X. Zhu and M. Heimlich, "High gain/power quotient variable-gain wideband low-noise amplifier for capsule endoscopy application," Microwave and Optical Technology Letters vol. 54 no. 11 pp. 2563-2565 2012.

[2] A. Iji X. Zhu and M. Heimlich, "A folded-switching mixer in SOI CMOS technology," Proc. IEEE MWSCAS pp. 458-461 Aug. 2012.

[3] A. Iji X. Zhu and M. Heimlich, "A 4.5mW 3-5 GHz low-noise amplifier in 0.25-um silicon-on-insulator CMOS process for power constraint application," Microwave and Optical Technology Letters vol. 55 no. 1 pp. 89-93 2013.

[4] A. Iji X. Zhu and M. Heimlich, "Low power high gain low noise amplifier (LNA) for ultra-wideband applications," Microwave and Optical Technology Letters vol. 55 no. 6 pp. 1399-1401 2013.

[5] A. Iji X. Zhu M. Heimlich and Y. Sun, "An OTA-C filter in SOI CMOS for UWB application," Proc. IEEE MWSCAS 2012.

[6] D. P. Madelo, A. Tayros, R. Sabarillo, A. Lowaton and J. Hora, "Design of Low Power P-Gated Schmitt Trigger SRAM in 65nm CMOS Technology," 2018 International Conference on Control, Electronics, Renewable Energy and Communications (ICCEREC), Bandung, Indonesia, 2018, pp. 189-194, doi: 10.1109/ICCEREC.2018.8711999.

[7] Zhu, Xi & Sun, Y.. (2009). Low-distortion low-voltage operational transconductance amplifier. Electronics Letters. 44. 1434 - 1436. 10.1049/el:20081301.

[8] P. Singhanath, A. Suadet, A. Kanjanop, T. Thongleam, S. Kuankid, and V. Kasemsuwan, "Low voltage adjustable cmos schmitt trigger," in 2011 Fourth International Conference on Modeling, Simulation and Applied Optimization. IEEE, 2011, pp. 1–4.

[9] K. Kim and S. Kim, "Design of schmitt trigger logic gates using dtmos for enhanced electromagnetic immunity of subthreshold circuits," IEEE Transactions on electromagnetic compatibility, vol. 57, no. 5, pp. 963–972, 2015.

[10] Z. Wang, "Cmos adjustable schmitt triggers," IEEE Transactions on instrumentation and Measurement, vol. 40, no. 3, pp. 601–605, 1991.

[11] C. Zhang, A. Srivastava, and P. Ajmera, "Low voltage cmos schmitt trigger circuits," Electronics letters, vol. 39, no. 24, pp. 1696–1698, 2003.

[12] Z. Chen and S. Chen, "A high-speed low voltage cmos schmitt trigger with adjustable hysteresis," in 2017 IEEE/ACIS 16th International Conference on Computer and Information Science (ICIS). IEEE, 2017, pp. 293–297.

[13] B. Dokic, "C. m. o. s. schmitt triggers," in IEE Proceedings G. Electronic Circuits and Systems, vol. 131, 1984, pp. 197–202.

[14] I. Filanovsky and H. Baltes, "Cmos schmitt trigger design," IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications, vol. 41, no. 1, pp. 46–49, 1994.

TABLE I
COMPARISSON WITH OTHER WORKS

Prior Study	*Technology Node*	*Supply Voltage*	*Hysteresis*	*Technique*	*Type of Schmitt*	*Transistor Count*	*Power Consumption*	*Critical Review*
[8]	180 nm	0.4 V	Adjustable	Dynamic Body Bias	Low Power	6	0.13 uW	Hysteresis is adjustable and lower technology node compared to [11]
[9]	130 nm	0.4 V	Fixed	DTMOS	Low Power	6	* *	Faster switching speed but power consumption is increasing if hysteresis will increase
[11]	1.5 um	<1V	Fixed	Dynamic Body Bias	Low Power	4	195 uW	Hysteresis is not adjustable but uses Dynamic body bias for faster switching
[12]	40 nm	>1V	Adjustable	Adjustable Body Bias	Low Power	6	40 uW	Adjustable Hysteresis using VTMOS with drawback in terms of leakage current
[18]	3 um	*	Fixed	No Hysteresis Biasing	High Power	5	1.17 mW	The hysteresis is dependent on device dimensions, process parameters, and supply voltage, despite being fixedly biased
[26]	90 nm	1.2 V	Fixed	Conventional	Layout design	6	* * *	Fixed hysteresis based on [16] and focused on layout improvement
This Work	22 nm FDSOI	0.4 V	Adjustable	Gate Controlled Adjsutable Hysteresis	Low Power	8	in terms of nW - pW	Small Hysteresis window provides precise and reliable switching, minimizing false triggering and ensuring stable operation.

*NA. **proportional to the hysteresis width. ***NA.

[15] M. Janveja, A. Khan, and V. Niranjan, "Performance evaluation of subthreshold schmitt trigger using body bias techniques," in 2016 International Conference On Computational Techniques In Information And Communication Technologies (ICCTICT). IEEE, 2016, pp. 486–489.

[16] M. Maymandi-Nejad and M. Sachdev, "Dtmos technique for low-voltage analog circuits," IEEE transactions on very large scale integration (VLSI) systems, vol. 14, no. 10, pp. 1151–1156, 2006.

[17] A. Aggarwal, "The use of hysteresis with comparators and how it affects functionality," https://resources.pcb.cadence.com/blog/2020-the-use-of-hysteresis-with-comparators-and-how-it-affects-functionality, May 2013.

[18] M. Steyaert andW. Sansen, "Novel cmos schmitt trigger," Electronics Letters, vol. 4, no. 22, pp. 203–204, 1986.

[19] Y. Kosasayama, Y. Arima, M. Ueno, M. Kimata, K. Himei, and T. Asano, "Differential voltage (δV) comparator with variable channel-size mosfet," IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, vol. 87, no. 2, pp. 357–363, 2004.

[20] V. Katyal, R. L. Geiger, and D. J. Chen, "Adjustable hysteresis cmos schmitt triggers," in 2008 IEEE International Symposium on Circuits and Systems. IEEE, 2008, pp. 1938–1941.

[21] V. Pedroni, "Low-voltage high-speed schmitt trigger and compact window comparator," Electronics Letters, vol. 41, no. 22, p. 1, 2005.

[22] A. Suresh, "A low power schmitt trigger design using sbt technique in 180nm cmos technology," in 2014 IEEE International Conference on Advanced Communications, Control and Computing Technologies. IEEE, 2014, pp. 533– 536.

[23] M. Hosseinnejad, A. Erfanian, and M. A. Karami, "On the design of low power cmos schmitt trigger for biomedical application," in 2019 27th Iranian Conference on Electrical Engineering (ICEE). IEEE, 2019, pp. 1756–1760.

[24] P. Gupta, A. B. Kahng, P. Sharma, and D. Sylvester, "Gate-length biasing for runtime-leakage control," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 25, no. 8, pp. 1475–1485, 2006.

[25] S. Narendra, D. Antoniadis, and V. De, "Impact of using adaptive body bias to compensate die-to-die vt variation on within-die vt variation," 02 1999, pp. 229– 232.

[26] G. A. Raza and R. Mehra, "Area and power efficient layout design of schmitt trigger," in 2015 International Conference on Computer, Communication and Control (IC4). IEEE, 2015, pp. 1–4.

[27] J. A. Hora, X. Zhu and E. Dutkiewicz, "Simplified Over- Temperature Protection Circuit Structure for WSN/IoT Device Power Management," 2019 13th International Conference on Sensing Technology (ICST), Sydney, NSW, Australia, 2019, pp. 1-4, doi: 10.1109/ICST46873.2019.9047726.

[28] J. R. Otadoy, K. Genesis Jimenez, J. A. Hora, R. -A. Cristine O. Calimpusan and A. C. Lowaton, "Analysis and Comparison of Novel Clock Gating Cell Topologies in 65nm CMOS Process Technology," 2019 IEEE 11th International Conference on Humanoid, Nanotechnology, Information Technology, Communication and Control, Environment, and Management (HNICEM), Laoag, Philippines, 2019, pp. 1-6, doi: 10.1109/HNICEM48295.2019.9073358.