A Soft Error Upset Recovery SRAM Cell for Aerospace and Military Applications

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***Abstract*— Space radiation particles causes malfunction in electric circuits. It is especially susceptible to memory-sensitive storage devices. When it affects data stored in the memory circuit, it causes disruption. Standard 6T SRAM is incapable of mitigating this disruption. Consequently, numerous authors presented various resilience strategies. However, a trade-off exists between memory cell efficiency and soft error probability. This article describes a polar design soft error upset recovery SRAM memory cell (SUR-16T) that effectively recovers lost data due to a high-energy particle strike. SUR-16T has superior write stability, lower hold power dissipation, and shorter write access time at PVT variations compared to the mentioned memory cells. Furthermore, SUR-16T has a 0.96x/ 1.15x/ 1.10x/ 1.18x/ 1.02x/ 1.64x greater critical charge than SEA-14T/ RHBD-13T/ RHMC-12T/ QCCS-12T/ NRHC-14T/ HRRT-13T at 0.8V. In addition, the proposed memory cell demonstrated a higher relative figure of merit than existing memory cells.**

***Clinical relevance*— This paper demonstrates a radiation-hardened SRAM circuit that exhibits a higher critical charge when it is impacted by a high-energy charged particle with a LET of >10MeV-cm^2/mg.**

I. INTRODUCTION

Artificial shuttles and spacecraft are growing more common in space exploration. Spacecrafts were made up of thousands of electrical components. Furthermore, the space radiation environment was highly vulnerable to these electrical components [1]. According to [2], small energy space radiation particles, like α particles, can harm electronic components. Soft errors from radiation particles to electronic components have been critical in aerospace applications for over half a decade. As a result, numerous aviation and electronic engineering researchers explore radiation factors, radiation impacts on electronic components, and techniques to defend against or adapt to radiation. Exposing an electronic component or system to radiation is known as radiation hardening. If it reduces the influence of radiation, it is said to be radiation hardened. Understanding radiation effects is necessary to make radiation resistant components.

NASA study shows that space radiation anomalies could damage the spacecraft electronics [3]. The radiation particle's direct or indirect ionization to the electronic component causes disruptions in the electric field and creates a transient pulse over the sensitive area. If accumulated charge surpasses a MOS device's critical charge, the whole structure malfunctioned [1],[4]. This malfunction procedure was stated as single event upset (SEU), and it is more susceptible to stored memory device data [3].

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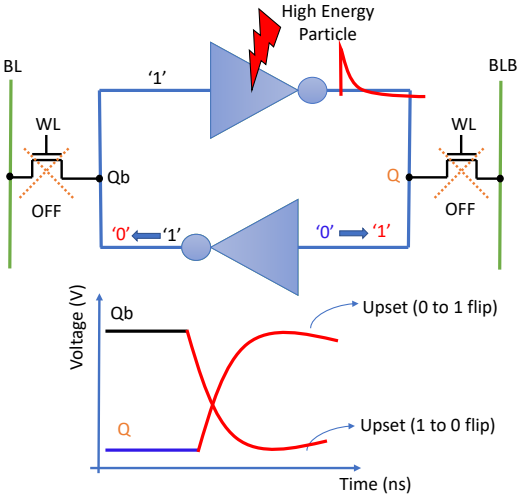

Fig. 1. Upset issue of conventional SRAM cell due to high energy particle strike

SRAM memories comprise a significant portion of the system-on-a-chip (SoC); therefore, chip designers shorten SRAM transistors to increase memory density. Shrinking transistors are highly susceptible to threshold voltage fluctuations and a soft error rate [5]. The radiation particle hits are more vulnerable to reverse-biased drain regions in SRAM memory. As depicted in Fig. 1, a high-energy radiation particle contacts the SRAM memory-sensitive node and creates an ion track inside the memory cell, upsetting the storage node [6]. Thus, high-energy radiation particles disrupted conventional 6T SRAM memory [7]. Radiation-hardened methods have emerged during the last 30 years. Our literature study verified various mitigation approaches like system level mitigation (error correction code (ECC), triple modular redundancy (TMR)), layout level mitigation, and circuit level mitigation (RHBD) hardening methods in [8]. According to the Rockett et al. [9] typical CMOS foundries make circuit-level mitigation easy to develop and validate. Thus, we concentrated on modern unique circuit-level radiation-resistant SRAM memory cells, including SEA-14T[10], RHBD-13T [11], RHMC-12T [12], QCCS-12T [13], NRHC-14T [14], and HRRT-13T [15].

These designs have a trade-off between soft error probability and memory cell performance. Hence, this paper describes a soft error upset recovery 16T SRAM cell (SUR-16T) as an alternative to the existing memory cells limitations.

This paper is organized as follows: Section II states the state-of-the-art for existing radiation-hardened SRAM memory cells. Section III describes the proposed soft error upset recovery 16T SRAM cell (SUR-16T) fundamental

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working and soft error recovery analysis. Moreover, Section IV experimentally investigates the performance metrics of all existing and proposed memory cells and comparison. Finally, Section V is a conclusion.

II. State-Of-The-Art of Existing Radiation Hardened Memory Cells

This section describes state-of-the-art of recent unique radiation hardened memory cells i.e., SEA-14T[10], RHBD-13T [11], RHMC-12T [12], QCCS-12T [13], NRHC-14T [14], and HRRT-13T [15].

The reliable soft-error-aware 14T SRAM memory cell (SEA-14T) consists of four storage nodes. Two storage nodes are primary, while the other two are secondary nodes, which allows the recovery of lost data from the primary storage nodes [10]. This design mitigates soft errors at all the sensitive nodes, but its read access time is challenging due to reduced read current.

Another radiation-resistant memory cell was RHBD-13T. In RHBD-13T, authors added two always on NMOS transistors (N1, N2) and N5, another access transistor with separate control signals RWL and RBL to increase memory cell read and write stability. This design mitigates upset problems in all sensitive nodes [11]. The major drawback of the RHBD-13T memory cell is its more static power dissipation when it is in hold mode, which can increase cell's total power consumption.

The RHMC-12T design follows a new polar approach to reduce sensitive nodes count in the memory cells. Moreover this design mitigates upset issue in all storage nodes effectively [12], but the write access time was higher due to longer feedback path to the primary to secondary storage nodes.

The QCCS-12T memory cell follows the cross-coupled outputs of each other to the inputs. The optimal strategy is determined by its read and write capability [13]. This design also mitigates upset issues in all sensitive storage nodes, and this design's only shortcoming is its low critical charge.

Another unique radiation resistant design was NRHC-14T. This design also follows polar strategy to reduce number of sensitive nodes. NRHC-14T mitigates upset issue in all sensitive storage nodes, but the major problem with this design is its hold power and read access time [14].

The HRRT-13T was another radiation hardened design to mitigate upset issue. HRRT-13T added additional N5, N6, and N7 transistors to improve read access time [15]. But unfortunately, write stability of the memory cell degrades. As a result write access time got increased.

By considering the recent radiation hardened memory cells limitations, we mentioned a soft error upset recovery SRAM cell (SUR-16T) that mitigates upset issues along with improved performance metrics of the memory cell. The technical specifications of proposed SUR-16T memory cell has follows:

1) The SUR-16T memory cell recovers all sensitive storage nodes and node pairs stored data when they impacted with high energy radiation particle.
2) The proposed SUR-16T write ability and the hold static power dissipation improved even considering PVT variations.
3) SUR-16T memory cell provides higher effective critical charge (Q_{Crit}) compared to the existing memory cells at 0.8V supply voltage.
4) Finally, SUR-16T exhibits a higher figure-of-merit by considering effective electric quality metric (EQM) factor.

III. SUR-16T Memory Cell Basic working and Soft Error Recovery Analysis

This section describes the read, write, and hold operations of the proposed SUR-16T memory cell in detail; furthermore, it describes the SUR-16T soft error recovery analysis at all sensitive nodes of a memory cell. Figures 2 and 3 depict the proposed SUR-16T memory cell design and thin-cell layout structure.

A. Proposed SUR-16T Memory Cell Basic Working

The SUR-16T memory cell comprises four storage nodes with 8 PMOS and 8 NMOS transistors. I0 and I1 are the main storage nodes; I2 and I3 are redundant. I2 and I3 storage nodes are also named recovery storage nodes. We examined polar design to decrease memory cell-sensitive nodes. In this polar design, transistors N7, N1 shares storage node I0 and N2, N8 shares I1 storage node. If the proposed SUR-16T memory cell is at logic '1', storage nodes I0, I1, I2, and I3 store '1', '0', '1', and '0', respectively.

The working of hold mode operates when wordline was disable i.e., WL=1 and BL, BLB prechaged to supply voltage. Then transistors, N1, N3, N5, N8, P2, P6, P4 are in off condition and remaining transistors are in on condition results same data retrieved at the storage nodes.

The read operation was performed by enabling access transistors (WL=0), and the bit lines were precharged to the supply voltage. When SUR-16T stores the logic value '1', BLB discharges through the P8 and N2 transistors to the ground terminal until N1 transistor goes to ON condition. As a result, potential difference of bitlines detected by sense amplifier and exhibits a proper logic state at the output (not shown in paper).

To write a memory cell from logic '1' to '0', the word line must be enabled (WL=0), and the bit lines was connected to the ground and supply voltage, respectively. I0 discharges through N1, P7 and I1 charges through P8, N2 transistors. Thus, I0 and I1 deliver data to logic '0' and '1' since P4, P6, and N3, N5 transistors are in on and off conditions, respectively.

B. SUR-16T Soft Error Upset Recovery Analysis

As mentioned in the introduction, when a high-energy particle with an average energy of more than 10 MeV impacts the drain region of a reverse biased off transistor, due to drift, diffusion, and direct ionization, extra charge carriers are generated inside the transistor, causing a transient pulse across the drain area. According to the article [4], when a high-energy particle hits NMOS off-drain region, it generates a negative pulse, and the output is either 0 to 0 or 1 to 0. At the same time, PMOS generates a positive pulse that produces a 1 to 1 or 0 to 1 transient pulse [8].

If the SUR-16T memory cell is stored at logic '1', storage nodes I0, I1, I2, and I3 store '1', '0', '1', and '0' logic states,

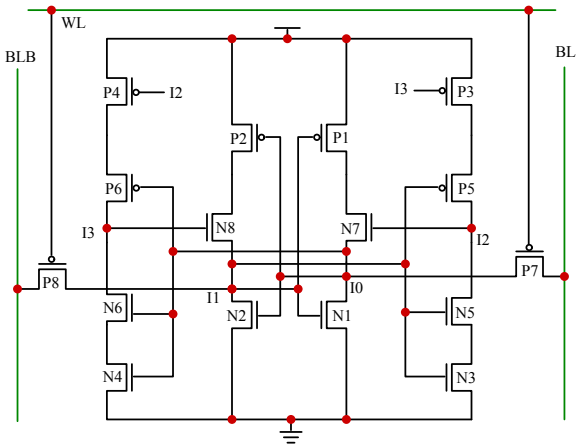

Fig. 2. Proposed SUR-16T memory cell Schematic

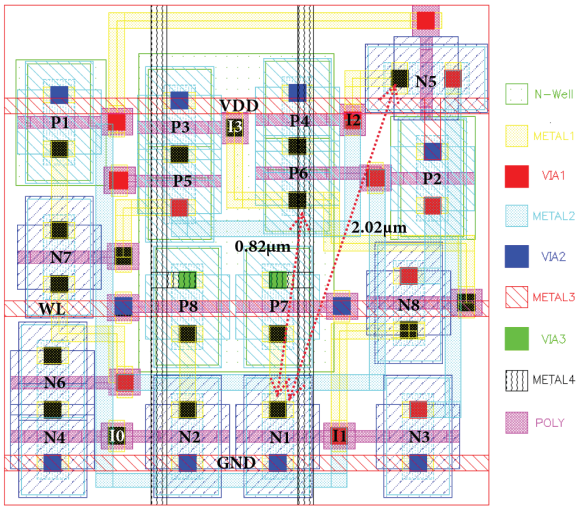

Fig. 3. SUR-16T memory cell thin-cell layout

respectively. The SUR-16T memory cell off transistors drain regions is considered sensitive nodes. Therefore, storage nodes I0, I2, and I3 are sensitive, as I1 was radiation-resistant because it had a negative pulse. The individual sensitive nodes' upset recovery process is shown as follows:

1) Soft error upset at I0 storage node: Storage node I0 data temporarily flips from logic '1' to '0' when a high-energy radiation particle hits the N1 off transistor. Thus, transistors N2, N4, N6 and P2, P6 momentarily switch off and on. I3 stored logic '0' turns N8 off, then I1 becomes high-impedance. According to [16], a high-energy particle's high impedance cannot alter the logic state and keep its original value. I2 stored logic '1' turns N7 on and I1 keeps 0 turns P1 on. As a result, I0 retrieves data from N7 and P1 transistors, as shown in Fig. 4, SEU @ I0 state.

2) Soft error upset at I2 storage node: Storage node I2 temporarily switches from logic '1' to '0' when a high-energy radiation particle hits the N5 off transistor. Thus, transistors N7 switch off and P4 switch on. I0 is in high impedance when N1 and N7 transistors are off. Initially, I3 and I1 stored logic '0', causing I2 to recover its logic '1' state. This is shown in Fig. 4, SEU @ I2 state.

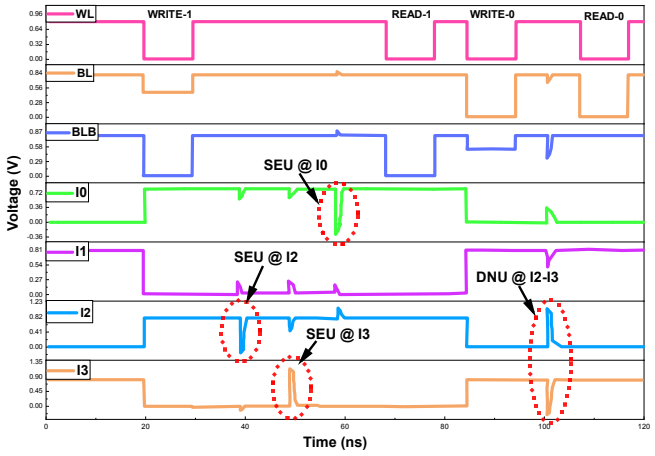

Fig. 4. Soft error upset recovery transient analysis of SUR-16T memory cell

3) Soft error upset at I3 storage node: When a high energy radiation particle strikes the P6 off transistor then storage node I3 stored data temporarily flips from logic '0' to '1'. Then N8 turns to on and P3 turns to off. This doesn't effect any other storage nodes of the memory cell. As I0 stored logic '1' causes N4 and N6 always on makes I3 recover back to logic '0'. This is shown in Fig. 4, SEU @ I3 state.

4) Soft error upset at I2 and I3 storage node pairs: According to the article [17], when we go beyond the deep sub-micron technology node transistors used in radiation hardened applications, leads to charge sharing issue between the closest sensitive node pairs. So, we consider sensitive node pairs also impact with radiation particle strike.

Storage nodes I2 and I3 momentarily switch from logic '1' to '0' and '0' to '1', respectively, when a high-energy radiation particle hits the N5 and P6 off transistors. Thus, transistors N7, P3 switch off and N8, P4 switch on. I0 and I1 storage nodes are unaffected. As I0 initially stored logic '1' makes I3 back to logic '0' further, I1 and I3 make P3, P5 on. This state recovers I2 back to logic '1'. This is shown in Fig. 4, double node upset (DNU) @ I2-I3 state.

High-energy particles flip storage node pairs I0-I2 and I0-I3. This may flip initial bits in other storage nodes. Any sensitive storage node pair with less than or equal to 2 μm area and 0.6 μm area between two NMOS and NMOS to PMOS transistors has charge sharing issue [8]. Hence, a 2.02 μm between I0 and I2 and 0.82 μm between I0 and I3 was maintained in the layout design (in Fig. 3) to minimize the charge-sharing issue.

The probability of two or more storage nodes simultaneously flipped due to single high energy ion strike is low. If this happen, charge dispersion spread across the other nearer storage nodes.

IV. Memory Cell Performance Metrics Analysis and Comparison

In this section we discuss stability, access time, hold static power consumption, critical charge and overall performance metric figure-of-merit (FOM) analysis and comparisons. All the simulations are performed by using UMC 65nm CMOS technology node.

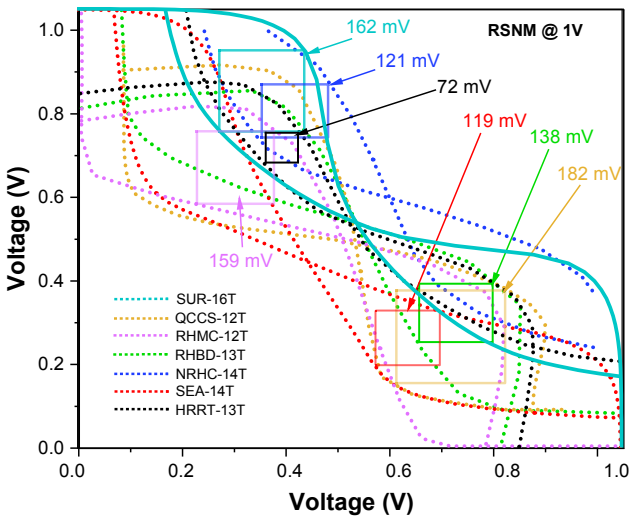

Fig. 5. Comparison of all radiation hardened memory cells RSNM

A. Stability

Static noise margin (SNM) determines memory cell stability. SNM was the memory cell's minimal voltage without changing its storing state. Applying an external voltage source across the primary storage node and observing the voltage transfer characteristics of the two primary nodes creates a butterfly curve for read SNM (RSNM). RSNM of a memory cell is the biggest square that fits inside the smallest butterfly curve lobe [6].

RSNM generally depends on memory cells' cell ratio (CR) [18]. It is defined as the dimension of the driver to access the transistor. A constant CR value of 2 was considered for all memory cells' RSNM analysis. Figure 5 illustrates each memory cell's RSNM butterfly curves and smallest lobe square voltage values. QCCS-12T has the highest RSNM at a 1V supply voltage among the memory cells listed. Following QCCS-12T, SUR-16T reports a 162mV RSNM.

Memory cell write margins are measured by bit line margin (BLM) and word line sweep margin (CWLM). Sweeping BLB from VDD to GND and measure I0 storage node voltage determines the bit line margin (BLM). If BLB was completely discharged, but no flip at the I0 signals indicates a write failure. The word-line margin is detected at the storage node I1 when the word line sweeps from VDD to GND. If storage node I1 was not flipped, reported as a failed write margin.

A Monte-Carlo 1000-step simulation using a Gaussian Distribution function at ± 3 sigma level variations computed BLM, and CWLM write margins of all memory cells. BLM and CWLM mean (μ), and standard deviation (σ) values for all memory cells with a constant 1V supply demonstrate the variability. Table I evaluates all existing and proposed memory cell write margin mean, standard deviation, and variability ($\frac{\sigma}{\mu}$). Due to perfect write logic '0' and '1', SUR-16T has a better write margin and lower variability than other radiation-hardened memory cells. The RHMC-12T and HRRT-13T fail the CWLM write stability test because storage node QB does not flip.

TABLE I
COMPARISON OF WRITE MARGIN VOLTAGES USING BLM AND CWLM METHODS

	BLM			CWLM		
Design	μ	σ	$\frac{\sigma}{\mu}$	μ	σ	$\frac{\sigma}{\mu}$
SEA-14T	248.3	32.45	0.13	254.8	33.28	0.13
RHBD-13T	286.6	33.8	0.11	299.4	38.15	0.12
RHMC-12T	272.4	34.6	0.12	Fail	-	-
QCCS-12T	292.5	32.71	0.11	318.2	35.31	0.11
NRHC-14T	289.8	32.27	0.11	303.6	36.43	0.12
HRRT-13T	273.9	37.32	0.13	Fail	-	-
SUR-16T	298.2	31.6	0.10	306.7	30.28	0.1

B. Access Time and Hold Static Power Dissipation

Read/write access time determines a memory cell's performance[19]. Read access time (RAT) defined the time between WL reaching half of VDD and bit lines having a minimum 50mV voltage difference [20]. Write access time (WAT) defined the time from 50% of word line voltage to both primary storage nodes intersecting time [21]. According to the article [20], these access times are subject to PVT fluctuations; thus, we validated all specified memory cell's read and write access time under distinct VDD values (0.6 to 1V), temperatures (-45^{0}C to 125^{0}C), and threshold voltages (0.05 to 0.09). Due to a more significant driving current, QCCS-12T has a lower RAT, as shown in Fig. 6(a–c). SUR-16T has a lower RAT after QCCS-12T.

Whereas, for write access time almost all memory cells exhibits similar write access time at PVT variations except HRRT-13T, as shown in Fig. 6 (d), (e), and (f). This is due to HRRT-13T have separate read control signal. As a result it consumes more time to write the stored data.

Static power consumption is another reliable memory cell parameter. The hold static power of a memory cell is the maximum power consumed when the memory cell was in hold mode. Latch inverter and bit-line leakage power determines the hold power. According to [8], process variables affect this hold power most in space applications. Thus, a Monte-Carlo 2000-step simulation using a Gaussian Distribution function at ± 3 sigma level of variation demonstrated that all memory cells hold power. In Fig. 7, the suggested SUR-16T memory cell has a mean hold power of 23.34 pW. The SUR-16T has 2.48x/ 2.92x/ 1.06x/ 1.2x/ 2.66x/ 2.38x times lower hold power than SEA-14T/ RHBD-13T/ RHMC-12T/ QCCS-12T/ NRHC-14T/ HRRT-13T.

C. Critical Charge Analysis

The minimum amount of charge collected at the sensitive node of a memory cell that causes a bit flip is stated as critical charge of a memory cell. This critical charge (Q_{crit}) was determined primarily by the magnitude and pulse width of the applied double exponential current source and ion track created time constant of the memory cell. Q_{crit} was computed by using the following equation:

$$Q_{crit} = \int_0^{T_{crit}} I_{inj}(t)dt \quad (1)$$

Whereas, $I_{inj}(t)$ was the applied double exponential current pulse and T_{crit} stands for critical time.

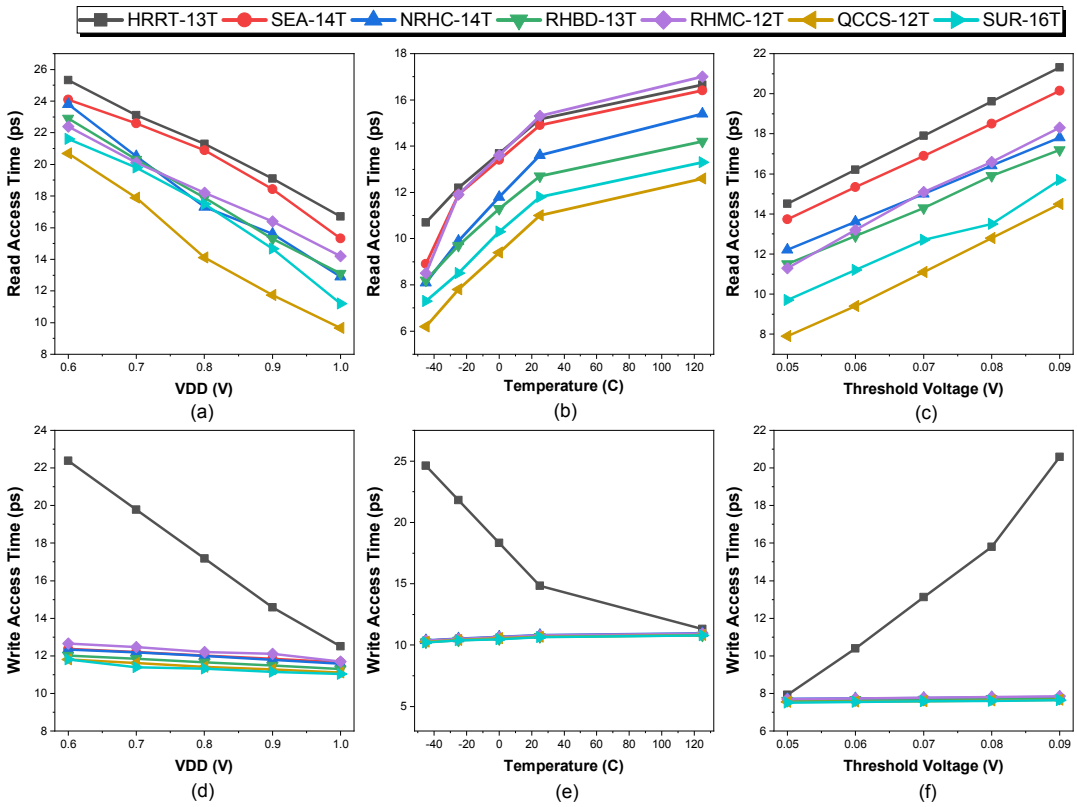

Fig. 6. Comparison of all radiation hardened memory cells access time under PVT variations (a) read access time varying with various VDD (b) read access time varying with various temperatures (c) read access time varying with various threshold voltages (d) write access time varying with various VDD (e) write access time varying with various temperatures (f) write access time varying with various threshold voltages

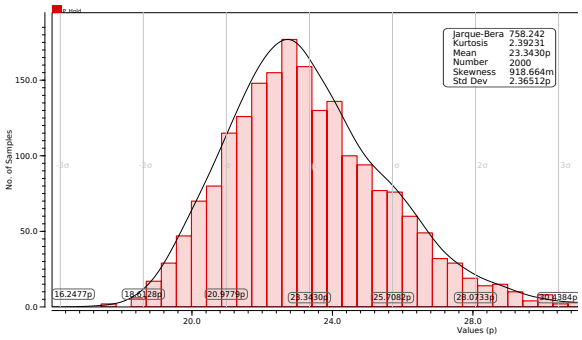

Fig. 7. SUR-16T hold power monte-carlo 2000-step simulation

$$I_{inj}(t) = I_{peak} * \left[exp\left(\frac{-t}{\tau_\alpha}\right) - exp\left(\frac{-t}{\tau_\beta}\right) \right] \quad (2)$$

Where $I_{inj}(t)$ is the current pulse injected at the sensitive node, I_{peak} is its peak amplitude which was depends on injected charge to the charge collection time constant, and τ_α and τ_β are the exponential curve's collected time and ion track-created time constants. We considered 200ps and 50ps of τ_α and τ_β values for a linear energy transfer (LET) of >10MeV-cm^2/mg. All memory cells Q_{crit} were estimated using (1) and (2).

The proposed SUR-16T exhibits a 75.6fC critical charge which was 0.96x/ 1.15x/ 1.10x/ 1.18x/ 1.02x/ 1.64x times higher than SEA-14T/ RHBD-13T/ RHMC-12T/ QCCS-12T/ NRHC-14T/ HRRT-13T. According to the article [22] a small increasing in critical charge efficiently reduces the soft error rate of a memory cell.

D. Overall Performance Metric Figure-of-Merit (FOM)

The literature assessment and state-of-the-art of all provided memory cells demonstrate a trade-off between soft error upset probability and performance of memory cell [23]. This overall performance measures a memory cell's figure of merit (FOM). FOMs fill the memory cell trade-off problem, and the radiation-hardened memory cell FOM was calculated using the equation below.

$$FOM = \frac{Q_{Crit} * RSNM * BLM}{RAT * WAT * P_{hold}} \quad (3)$$

Equation (3) verifies all memory cell's figure of merit. The ratio of comparing memory cell FOM to SUR-16T FOM determined relative FOM. The existing memory cells, SEA-14T/ RHBD-13T/ RHMC-12T/ QCCS-12T/ NRHC-14T/ HRRT-13T exhibits 0.163/ 0.20/ 0.57/ 0.9/ 0.22/ 0.06 value of relative FOM compared to the proposed SUR-16T memory cell. Higher relative FOM memory cells are more precise and ideal for all aerospace and military applications [23].

V. Conclusion

This paper presents a soft error upset recovery 16T SRAM cell (SUR-16T), resilient to high-energy radiation particles at all sensitive nodes and node pairs, by adopting a polar design strategy. The SUR-16T memory cell exhibits symmetric butterfly lobes for RSNM and a higher write noise

margin for the BLM and CWLM methods under ±3 sigma threshold variations. In addition, the write access time and hold static power dissipation at PVT variations were reduced. Higher critical charge and relative FOM values are the most significant aspects of the paper. Therefore, the proposed SUR-16T SRAM cell is suitable for all reliable aerospace and military memory applications.

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