22nm FDSOI Forward Body Biasing in Designing Ultra-Low Power, High PSRR Voltage Reference for IoT Power Management Applications

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***Abstract*—This paper presents a novel approach to voltage reference design, harnessing the bulk biasing technique in 22nm Fully Depleted Silicon-on-Insulator (FDSOI) technology. The proposed architecture exhibits ultra-low power consumption of 95.28 nW while having a dissipating supply current of 157 nA and a high Power Supply Rejection Ratio (PSRR) of more than -100 dB, realized through an all-MOSFET construction where TC compensation of PTAT and CTAT voltage generators is adopted. A temperature coefficient of 22.22ppm/°C is achieved over wide temperature range from -45°C to 100°C with an output voltage V_{REF} of 351 mV. With the growing demand for efficient, low-power, and compact solutions in Internet of Things (IoT) power management, this development contributes a significant step forward in the domain.**

***Index Terms*—Forward Body Biasing, FDSOI Technology, ultra-low power, all-MOSFET, low-voltage, high PSRR, IoT power management**

I. Introduction

As the Internet-of-Things (IoT) sector continues to expand and evolve, the development of low-power, low-supply voltage devices is a critical priority [1]. IoT devices, due to their always-connected nature, are usually battery-operated, requiring designs that consume minimal power to extend battery life. Voltage references serve as critical elements in all modern analog and mixed-signal systems, particularly in the context of IoT devices. This component ensures that the device functions correctly by providing a constant voltage, regardless of changes in temperature, power supply variations, or circuit loading. Historically, voltage references were generated using Bipolar Junction Transistors (BJTs) and resistors. These components were used to create a bandgap reference, which provides a stable voltage close to the bandgap of silicon, typically around 1.2 V [2]. However, the demand for lower supply voltages in IoT devices exposes the limitations of these traditional voltage references. In particular, BJT-based bandgap references can struggle to start up and remain stable under the low voltage conditions often required by IoT devices.

To address these challenges, all-MOSFET voltage references have been proposed as a more suitable alternative. The advancement of all-MOSFET solutions for analog/mixed-signal, and RF applications has come a long way since the early 20s. Several prior works have demonstrated the great potential of CMOS technology [3]–[9]. In references [10]–[12], the voltage reference takes advantage of the dependent on temperature properties of MOSFETs, including the threshold voltage (VTH) and the gate-to-source voltage (VGS). The proportional to absolute temperature (PTAT) and complementary to absolute temperature (CTAT) voltages, conventionally generated by the CMOS threshold voltage, can be effectively produced by MOSFETs operating in the sub-threshold region. This methodology is further refined by utilizing the forward body biasing technique inherent to Fully Depleted Silicon-On-Insulator (FDSOI) technology [13], [14]. This technique permits dynamic control over the threshold voltage, thus enhancing the suppression of power supply variations and improving the stability of the voltage reference. This advancement, coupled with operating MOSFETs in the sub-threshold region, paves the way for more power-efficient and compact designs in the future. Compared to its traditional BJT-based counterparts, this approach operates at a lower voltage and consumes less power, aligning more closely with the requirements of IoT applications.

PSRR, or Power Supply Rejection Ratio, plays a crucial role in voltage reference design. Standard practices to boost PSRR typically entail a larger chip area and heightened power consumption. These involve strategies such as deploying additional amplifiers [15], employing long-channel length transistors, cascode structures, and supplemental gain stages [16], [17], but these come with associated trade-offs. The frequency compensation capacitor, which is often a bypass or decoupling capacitor, is a crucial measure to obtain high PSRR [18], [19]. Consequently, the challenge lies in finding a balanced approach that improves PSRR without significantly compromising other design aspects.

Utilizing the forward body biasing of 22nm FDSOI technology, this paper describes an low-power all-MOSFET with a high PSRR voltage reference. The voltage reference is comprised of only a self-biased cascode current mirror with a PTAT generator as an active load to provide a bias current with a positive temperature coefficient (TC) and an NMOS diode connected to generate the CTAT voltage. Adding a low-pass filter based on MOSFETs to the output to further optimized the PSRR.

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II. Principle of Operation

A. Forward Body Biasing of Fully Depleted Silicon-On-Insulator (FDSOI)

The principle of operation for back gate or forward body biasing in Fully Depleted Silicon-On-Insulator (FDSOI) technology revolves around the capability to control the threshold voltage (Vth) of a transistor. The structure of an FDSOI transistor includes a thin silicon layer (also known as the channel) on top of a buried oxide (BOX) layer, which separates the channel from the bulk silicon substrate below. Figure 1. shows the conventional vs. flip-well devices in FDSOI technology. Flip well is a Forward Body Biasing (FBB) in which the NMOS is over the N-well substrate, just as the PMOS is over the P-well substrate. FBB is applied by biasing the body, or the substrate (the back gate), of the transistor with a voltage higher than the source voltage. Back gate bias works with gate voltage. This shifts the energy bands in the transistor's silicon body and narrows the bandgap between the valence and conduction bands. By adjusting the body bias, you can effectively control the threshold voltage of the transistor, which in turn controls the leakage current and speed of the transistor. In a low-power application, controlling leakage current is particularly important because it reduces power consumption when the transistor is off. The resulting effect is an increase in the carrier mobility in the transistor's channel, allowing for faster switching speeds and thus enhancing the overall circuit performance.

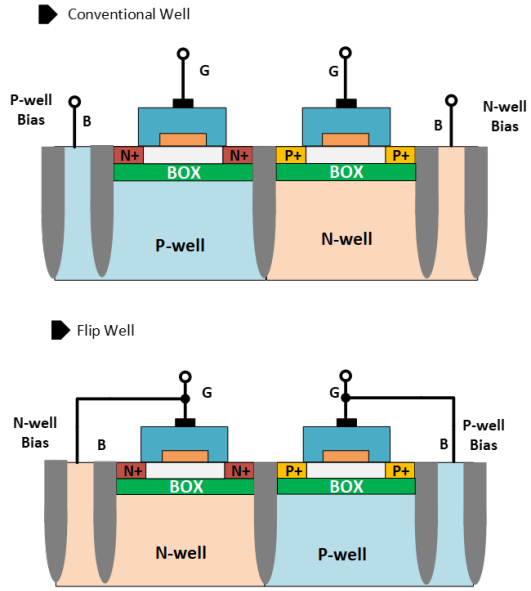

Fig. 1: Conventional well vs Flip-well

B. Proposed Voltage Reference with Bulk-Biasing Technique

The proposed ultra-low power, high PSRR, all-mosfet voltage reference with forward body biasing technique in 22nm FDSOI is shown in Fig. 2. The proposed design has four components: the start-up circuit, a self-biased cascode current mirror with a PTAT voltage generator as an active load, the CTAT voltage generator, and a MOSFET-based low-pass filter. All body of MOS transistors are connected to the device's gate terminal except for the MOSFET-based capacitors (M5 and MLP2).

a) Start-up Circuit: The start-up circuit is composed of M1–M5, where M2 and M4 are inverter circuits. The mosfet capacitor M5 having a low gate potential at the power-on stage will trigger the M2 and M3 to turn on, thereby generating a current that will feed to the current reference circuit, where the whole circuit system starts to work. Simultaneously, M1 begins charging the start-up capacitor M5. This charging process progressively turns off M2 and M3, effectively disconnecting the start-up circuit from the voltage reference's core to prevent unnecessary power loss.

b) PTAT Voltage Generator: As shown in Fig. 2, the PTAT voltage generator is connected to the self-biased cascode current mirror as an active load, and all body parts of the transistor are connected to the device's gate terminal. Assuming the current is in the range of nanoamperes (nAs), all MOSFETs are operating in a sub-threshold region, which is in the weak-inversion region, as shown in equation (1). The generation of PTAT voltage is composed of two transistors, M10 and M11, connected in series and capable of generating a PTAT voltage by making the size of M11 larger than M10. The V_{PTAT} is expressed in the equation below:

$$I_{\mathrm{D}} = \frac{W}{L}\mu C_{\mathrm{OX}} exp(\frac{V_{\mathrm{GS}} - V_{\mathrm{TH}}}{nVt})[1 - exp(-\frac{V_{\mathrm{DS}}}{Vt})] \quad (1)$$

$$V_{\mathrm{PTAT}} = V_{\mathrm{GS11}} - V_{\mathrm{GS10}} \quad (2)$$

$$V_{\mathrm{PTAT}} = n\frac{KT}{q} ln(\frac{\frac{W_{10}}{L_{10}}}{\frac{W_{11}}{L_{11}}}) + \Delta V_{\mathrm{TH}} \quad (3)$$

From equation (3), it is apparent that the first term dominates over the second. Given that V_{TH}, which exhibits a positive temperature coefficient, similarly features in the first term, we conclude that V_{PTAT} in equation (3) behaves as a PTAT (proportional to absolute temperature) voltage.

c) CTAT Voltage generator: The node to which the gate and drain of M14 were connected is where the CTAT (complementary to absolute temperature) voltage is taken. The M14 high-threshold n-channel MOSFET is used. Due to being a diode-connected M14, assume that the operating region is in the sub-threshold region given by equation (1), and the voltage characteristics are given by:

$$V_{\mathrm{CTAT}} = V_{\mathrm{GS14}} = V_{\mathrm{DS14}} \quad (4)$$

$$I_{\mathrm{D}} = \frac{W}{L}\mu C_{\mathrm{ox}} exp(\frac{V_{\mathrm{GS}} - V_{\mathrm{TH}}}{nVt})[1 - exp(-\frac{V_{\mathrm{DS}}}{Vt})] \quad (5)$$

$$V_{\mathrm{CTAT}} = V_{\mathrm{GS14}} = nV_{\mathrm{T}}[\frac{I_{\mathrm{D}}}{\frac{w}{L}\mu C_{\mathrm{ox}} V^2 T}] + V_{\mathrm{TH}} \quad (6)$$

d) Output V_{REF}: The output voltage of the PTAT voltage generator defined by V_{PTAT} is directly added to the voltage $V_{\mathrm{GS(CTAT)}}$) to obtain the output voltage V_{ref} as

$$V_{\mathrm{REF}} = V_{\mathrm{PTAT}} + V_{\mathrm{CTAT}} \quad (7)$$

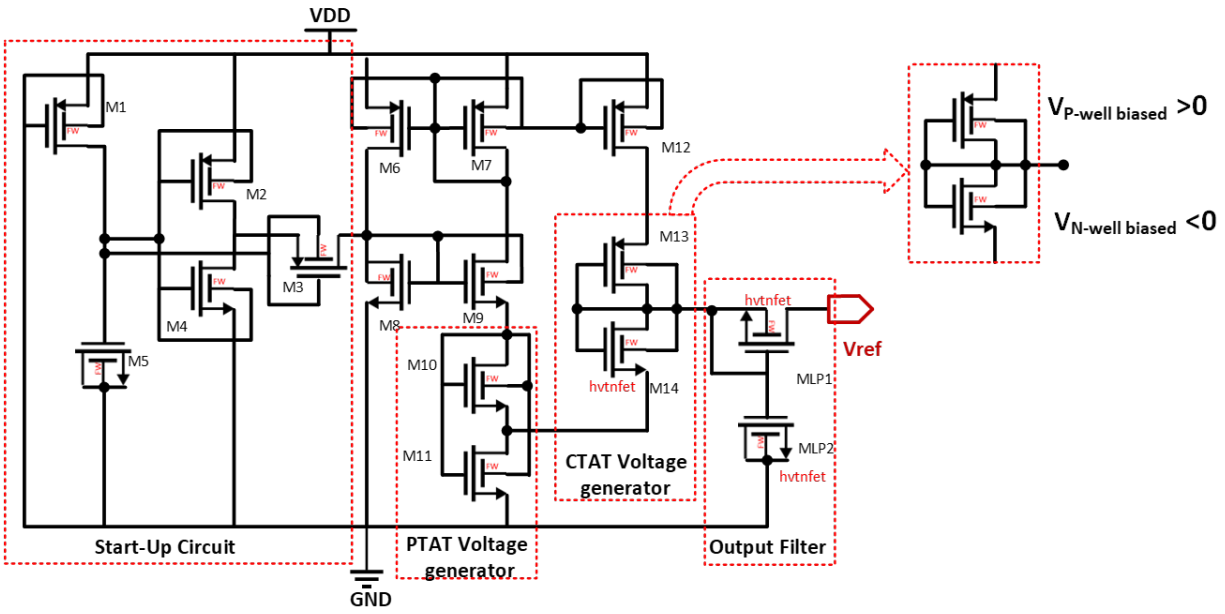

Fig. 2: Proposed Voltage Reference with Bulk-Biasing Technique

$$V_{\mathrm{REF}} = [n\frac{KT}{q} ln(\frac{\frac{W_{10}}{L_{10}}}{\frac{W_{11}}{L_{11}}}) + \Delta V_{\mathrm{TH}}] + [nV_{\mathrm{T}}[\frac{I_{\mathrm{D}}}{\frac{W}{L}\mu C_{\mathrm{ox}} V^2 T}] + V_{\mathrm{TH}}] \quad (8)$$

The first term in equation (8) represents the PTAT voltage, and followed by the CTAT voltage. By applying an appropriate weighting factor to these terms, it is possible to achieve a voltage reference with a near-zero temperature coefficient.

e) MOSFET-Based LPF: The two transistors added to the output are a mosfet-based low-pass filter. The gate-to-source voltage can change the resistance of the M15, which can function as a variable resistor. The M16 is a capacitor mosfet. In the simple low-pass RC filter, the MOSFET can take the place of the resistor together with the parasitic capacitance of C_{M16}, creating a RC filter that allows for dynamic gate-to-source voltage adjustment of the cutoff frequency.

III. Simulation Result

The proposed all-MOSFET with forward body biasing technique has been designed and simulated using Cadence Virtuoso with 22nm FDSOI technology. The circuit design is measured from -40°C to 100°C with output voltage V_{REF} 351mV at room temperature at a nominal voltage of 800mV. The process corner for SS and FF was also simulated and has a maximum output of 354 mV for the FF corner and a minimum voltage of 348 mV for the SS corner, with a temperature coefficient of 24.94ppm/°C for FF corner, 22.22ppm/°C for the TT corner, and 11.45ppm/°C for the SS corner, respectively, as shown in Fig. 3. The voltage reference, V_{REF}, was measured across 20 samples at the TT corner, yielding a 2% tolerance for the output voltage.

The line regulation performance of the proposed circuits with 20 samples at the TT corner is shown in Fig. 4. The result shows stability and accuracy across a supply range of 0.6 V to 1.2 V, with a measured line sensitivity of 0.862 %/V. This demonstrates the circuits' effectiveness in maintaining consistent output despite variations in the input supply voltage.

Fig. 5 shows the measured result of PSRR under VDD = 0.8 V with an ac voltage amplitude of 0.18 mV. The result

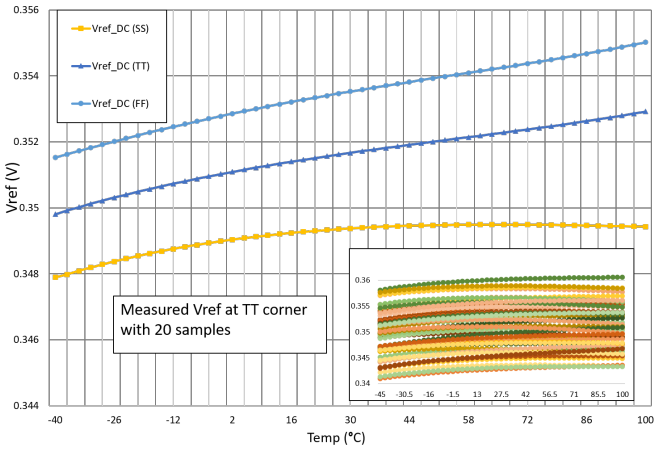

Fig. 3: Measured V_{REF} VS. Temperature for TT FF SS Corner with 20 samples at TT Corner

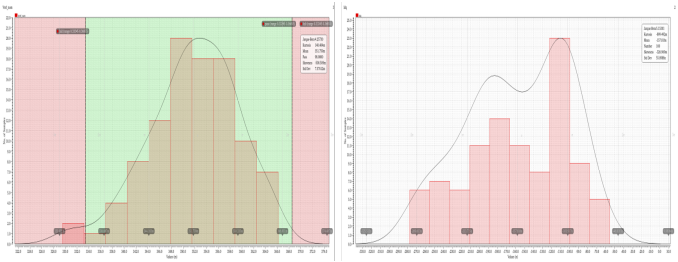

Fig. 4: Monte Carlo analysis for Vref and Quicient Current (Iq) with 100 iteration for SS TT FF Corner

TABLE I: Performance Comparison

Previous Work	*Technology Node*	*Supply Voltage (VDD)*	*Power (nW)*	*TC (ppm/°C)*	*V_{REF} (mV)*	*PSRR (dB)*	*LS (%/V)*	*Year*
[1]	180 nm	1.3	91	13.1	576	-74d@100Hz	0.02	2018
[2]	180 nm	0.8 - 1.6	37	42.1	240	-81@50Hz	0.85	2017
[10]	180 nm	0.5 - 2	15.65	46.2	344	-70@10Hz -51@100KHz -52@10MHz	0.25	2018
[12]	65 nm	0.8 – 1.2	1.32	105.51	420.57	-40@10Hz -66@100KHz -93@10MH	0.569	2022
[13]	65 nm	0.35 - 2 V	2.28	28	148	-53@100Hz	1.2	2019
This Work	**22 nm FDSOI**	**0.6 - 1.2**	**95.28**	**22.22**	**351**	**-93@100Hz -111@1KHz**	**0.863**	**2023**

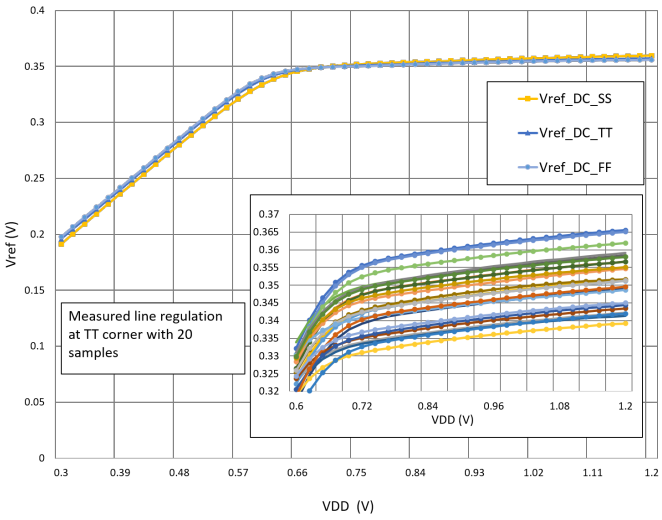

Fig. 5: V_{REF} vs. Supply Voltage (VDD)

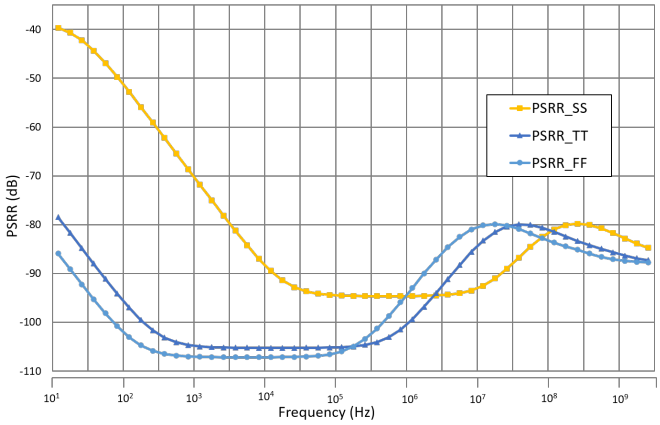

Fig. 6: Measured PSRR of proposed circuit at VDD=0.8 V

shows that the PSRR at 100 Hz for SS, TT, and FF corners is -48 dB, -93 dB, and -104 dB, respectively, and for 1KHz is around -67 dB, -111 dB, and -115 dB, respectively. The Monte Carlo analysis for output voltage V_{REF} and quiescent current is shown in Fig. 6, showing the result of process and mismatch variation. The yield of V_{REF} having a 5% tolerance is 100% for 100 iterations. The mean value of the quiescent current in the proposed circuit is 157.8 nA. Table I presents a detailed comparative evaluation of the proposed voltage reference's performance against other recent literature. Several key performance indicators such as temperature coefficient (TC), supply line sensitivity, variability in performance, power consumption, and power supply rejection ratio (PSRR) are considered in this analysis. Our proposed voltage reference design exhibits competitive performance across these parameters.

IV. Conclusion

This work presents an all-mosfet voltage reference that makes use of forward body biasing in 22nm FDSOI technology. With the addition of a mosfet-based low pass filter in the output stage, the proposed design achieves a high power supply rejection ratio (PSRR) of more than -100dB. Due to being operated in subthreshold region, it has a nano-watt power consumption and a reduced power supply voltage, which makes it suitable for low-power management IoT applications. The proposed design demonstrated robust results in terms of temperature coefficient (TC) over a broad

temperature range, line regulation, variation, Power Supply Rejection Ratio (PSRR), and power consumption. These attributes make our proposal a promising candidate for future energy-efficient and compact IoT devices.

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