Impact of Process-Induced Inclined Sidewalls On Small Signal Parameters of Silicon Nanowire GAA MOSFET

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***Abstract*— In this work, calibrated TCAD simulation results are used to examine the impact of process-induced inclined sidewalls on small-signal parameters of the nanowire (NW) gate-all-around (GAA) MOSFETs. The non-quasi-static (NQS) small-signal instead of the quasi-static (QS), parameters are extracted for better accuracy at higher operating frequencies. The distributed channel resistances (R_{gd} and R_{gs}) and the intrinsic terminal capacitances (C_{gd}, and C_{gs}) are susceptible to the inclination of sidewalls angle (θ). The increase in θ causes the distributed channel resistances to increase and the terminal capacitances to decrease.**

Keywords— gate-all-around NW MOSFETs, non-quasi-static (NQS), trapezoidal cross-section, small signal parameters.

I. INTRODUCTION

According to the 2023 International Roadmap for Devices and Systems (IRDS) [1], high-speed devices are essential for emerging technologies like 6G and driverless vehicles. Among the available architectures, nanowire (NW) Gate-all-around (GAA) MOSFET seems to be the most viable solution for designing high-speed hardware. The short channel effects (SCEs) play a significant role in sub 10 nm technology node but due to the high electrostatic control offered by the surrounding gates and smaller dimensions of channel widths makes gate-all-around architecture more immune to SCEs in comparison to the other geometric structures [2]. Nonetheless, due to photolithography's technological limitations at nanoscale dimensions, the rectangular channel cross-section of the NW GAA MOSFET device may eventually become a trapezoidal (Tz) or triangle during fabrication [3], [4]. The trapezoidal cross-section of the channel affects the device's characteristics and circuit performance. Moreover, the overall performance of the device is deviated from what is predicted which, poses reliability issues at such short-channel technology nodes [5].

Numerous types of research have been analyzed on the process-induced inclined sidewalls of FinFETs and NW GAA MOSFET [6-10]. Liu et al. [6] conducted a study on the channel cross-sectional dependence on short channel effects in fin-type double-gate metal oxide semiconductor field-effect transistors. Buhler et al. [7] investigated the trapezoidal SOI FinFET analog parameters' dependence on channel cross-section shape. Wu et al. [8] analyzed the impacts of nonrectangular fin cross-section on the electrical characteristics of FinFETs. Kumari et al. [9] proposed the effect of process-induced inclined sidewalls on the subthreshold modeling of GAA MOSFETs. Sato et al. [10] have studied the effects of the corner angle of trapezoidal and triangular channel cross-sections on the electrical performance of silicon nanowire field-effect transistors with semi-gate-around structures. However, reports on the effects of process-induced inclined sidewalls of the trapezoidal cross-section NW GAA MOSFETs on the small signal parameters are negligible.

The development of a precise small-signal equivalent circuit model holds paramount importance in enhancing the performance of NW GAA MOSFETs for high-frequency operation and expediting the circuit development process. In comparison to the quasi-static small signal model, the non-quasi-static (NQS) small signal model exhibits superior accuracy in capturing the device behavior up to one-third of the cut-off frequency [11], [12]. The NQS model adeptly accounts for the charging and discharging delays of the channel charge resulting from fluctuations in the terminal voltages [13].

Thus, the present study presents the impact of process-induced inclined sidewalls on the NQS small-signal parameters of NW GAA MOSFETs, supported by well-calibrated 3-D TCAD simulation results. The paper is structured as follows: Section II provides an overview of the device simulation framework, followed by Section III, which presents the findings and corresponding discussions. Lastly, Section IV concludes the study.

II. DEVICE FABRICATION AND SIMULATION FRAMEWORK

As detailed in Ref. [9], [14] NW GAA MOSFETs were manufactured at Taiwan Semiconductor Research Institute (TSRI). The simulated structure which closely matches the fabricated device structure is created using the structure editor tool available in TCAD Sentaurus. Fig. 1(a) illustrates the trapezoidal-shaped NW GAA MOSFETs with a translucent source. A high-k dielectric stack and a TiN metal layer surround the silicon channel area, which is mildly doped ($N_a = 10^{17}$ cm^{-3}). Arsenic with a concentration of 10^{20} cm^{-3} has been doped in the source/drain regions. The channel cross-section area of trapezoidal-shaped NW GAA MOSFETs is shown in Figures 1(b) and 1(c), which clarifies the side-wall inclination angle as 10° and 20° respectively. The Philips unified mobility model is used to address mobility variations concerning the different scattering mechanisms as well as different silicon plane orientations. SRH recombination and high-field saturation models were also taken into account during the simulations. TCAD was used to model three-dimensional (3D) NW GAA MOSFETs by extruding trapezoidal 2-D cross-sections and mirroring them with Sentaurus structure editor (SDE).

Figure 2 depicts the high-frequency NQS model for deriving small-signal characteristics from simulated Y parameters data of the trapezoidal NW GAA MOSFET. We used the extraction methods described as in [11], [12] for nanowire-based MOSFETs to extract the small-signal model parameters. Figures 3(a) and 3(b) shows the measured transfer characteristics (I_D-V_{GS}) and output characteristics (I_D-V_{DS}) of the device, respectively. These experimental data were employed to calibrate the simulation models and accurately replicate the same characteristics.

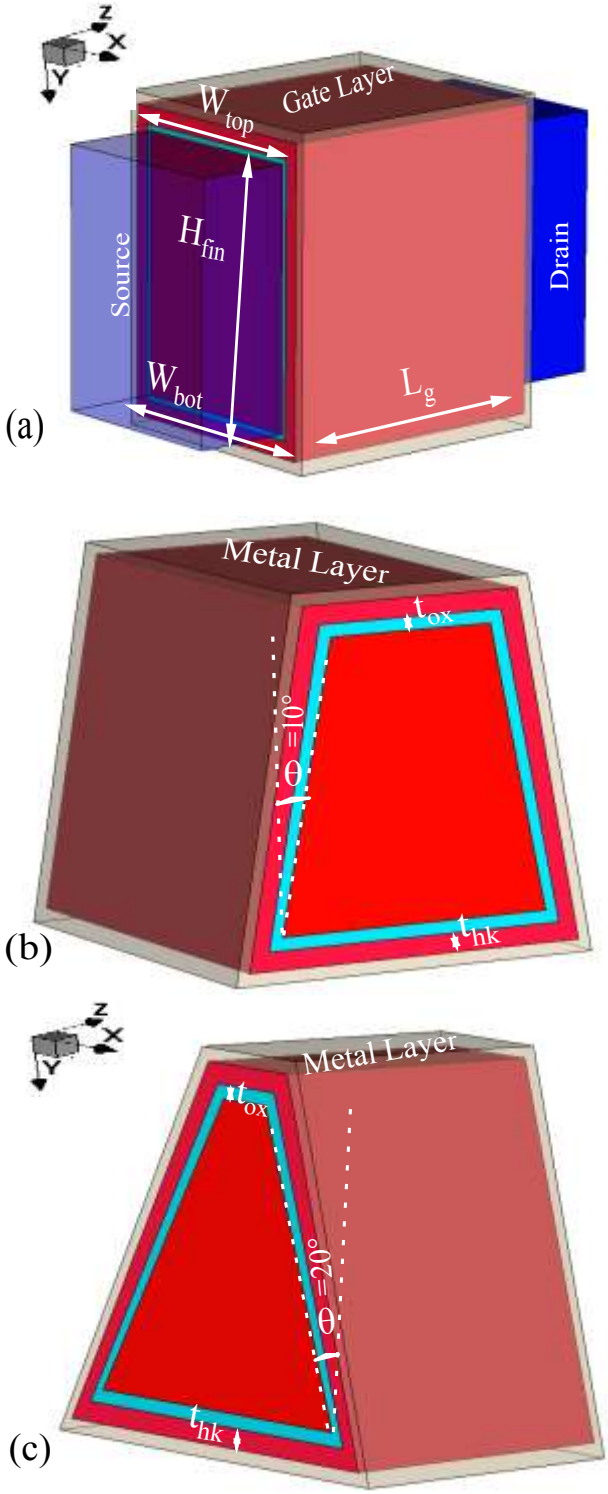

Fig. 1. (a) NW GAA MOSFETs reproduced in TCAD emulating the trapezoidal NW. and (b) Trapezoidal channel cross-section of NW GAA MOSFET with 10 degrees and (c) with 20 degrees.

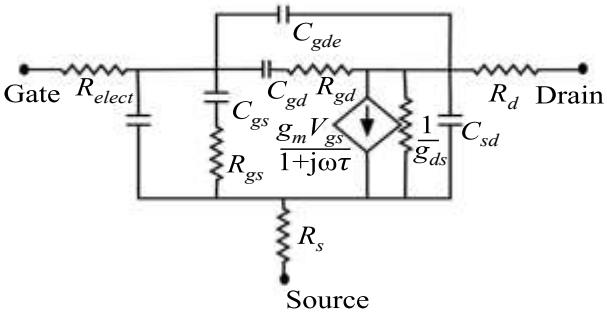

Fig. 2. NQS model of MOSFET operating in the saturation region, illustrating various capacitances (C_{gde}, C_{gse}, C_{gd}, C_{gs}) and distributed channel resistances (R_{gs}, R_{gd}). The model also includes important parameters such as the time constant (τ), transconductance (g_m), and output conductance (g_{ds}).

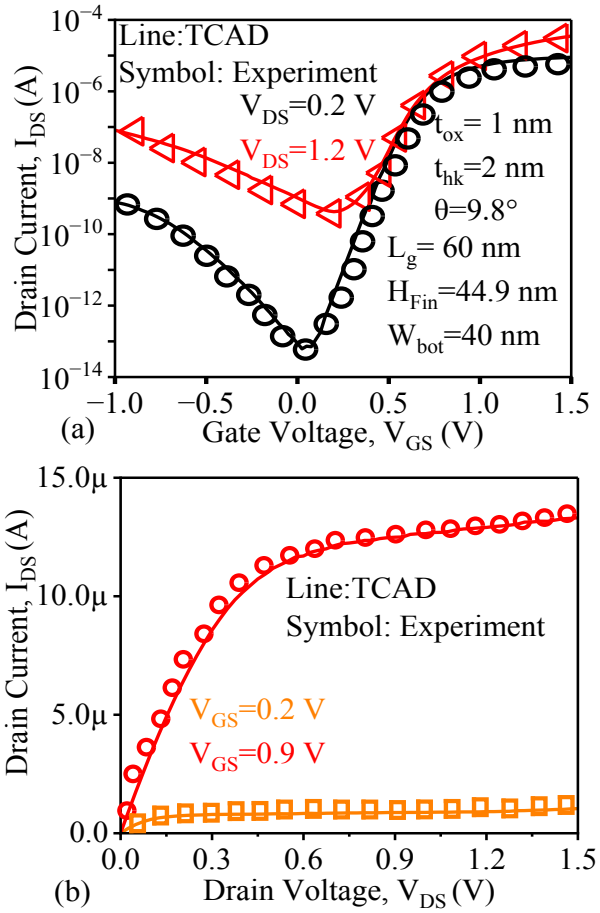

Fig. 3. Calibration of the TCAD model parameters to match the experimental (a) transfer and (b) output characteristics.

III. Results and Discussion

In this section, we present the impact of inclined sidewalls on the NQS small signal parameters of trapezoidal NW GAA MOSFETs. Fig. 4(a) shows the plot of the gate to drain capacitance (C_{gd}) concerning frequency, whereas the device bottom width is 10 nm and V_{gs}=V_{ds}=1V. It is observed that the C_{gd} remains constant up to 100 GHz and it starts decreasing at higher frequencies, which can be attributed to the inability of the transistor to create the variation in the inversion charge density corresponding to changing gate

voltage at the channel oxide interface under very high frequencies operating conditions. Fig. 4(b) demonstrates the impact of inclined sidewalls on the C_{gd}. The C_{gd} is measured at a frequency of 50 GHz for V_{gs} and V_{ds} of 1V. A decrement of almost 13% has been observed when an inclination angle of sidewalls (θ) is increased from 0° to 20° at W_{bot} = 10 nm. Furthermore, when W_{bot} is increased to 15 nm, for the similar

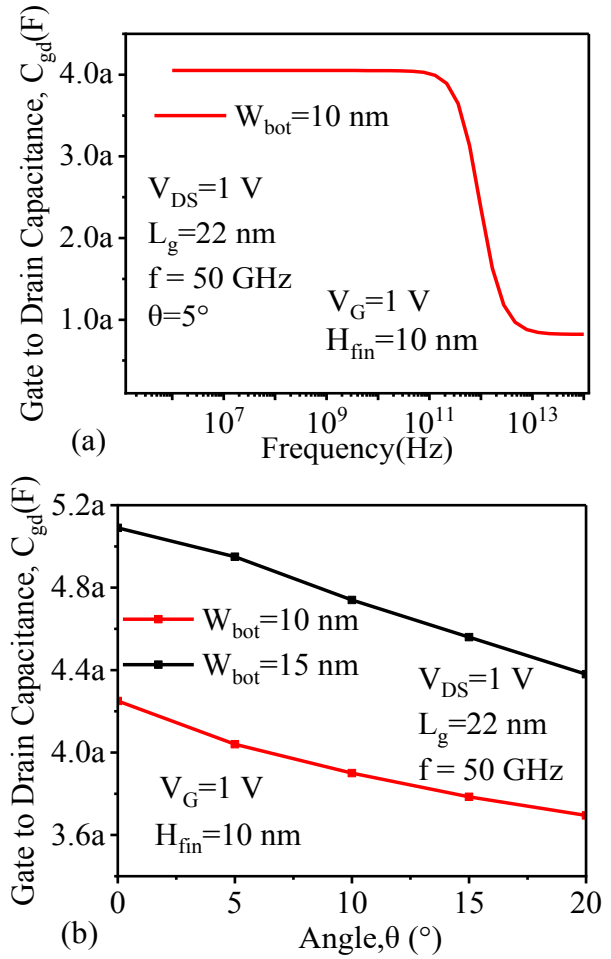

Fig. 4. Simulation results of (a) Gate to drain capacitance concerning the frequency and (b) impact of inclined angles on C_{gd} for different device bottom widths.

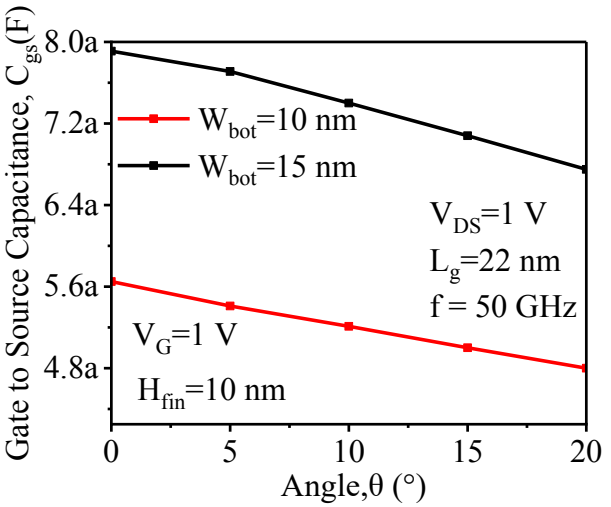

Fig. 5. Simulation results of the impact of inclined angles on Gate to Source capacitance at a frequency of 50 GHz for different device bottom widths.

variation in the inclination angle (0° to 20°), a 14% reduction of C_{gd} has been observed. The rise in the inclination angle results in a reduction of the overall cross-section area of the channel which leads to a decrease in the capacitance. When the bottom width of the device is increased, the channel cross-section area of the device increases, resulting in larger capacitance. A Similar variation in the gate-to-source capacitance has been observed in Fig. 5. Up to 15% (16%) decrement is observed in C_{gs} when θ is increased from 0° to 20° at W_{bot} = 10 nm (15 nm).

Fig. 6 (a) shows the gate-to-drain resistance (R_{gd}) concerning change in frequency. It observed that R_{gd} remains constant up to the cut-off range frequencies and it starts decreasing when the operating frequency crosses the cut-off frequency. Fig. 6(b) presents the impact of θ on the R_{gd}. It has been observed that R_{gd} rises for the rise in θ. The rise in R_{gd} can be attributed to decreasing channel cross-section area with the rise in θ. The R_{gd} is increased by 39% and 38% for a rise in θ from 0° to 20° at W_{bot} = 10 nm and 15 nm, respectively, at the frequency of 50 GHz. Similarly, Fig. 7 depicts the impact of θ on gate-to-source resistance (R_{gs}). For W_{bot} = 10 nm, R_{gs} climbs by almost 34% as θ varies from 0° to 20°. Similarly, at W_{bot} = 15 nm, R_{gs} increases by almost 32% as θ varies from 0° to 20° at the operating frequency of 50 GHz.

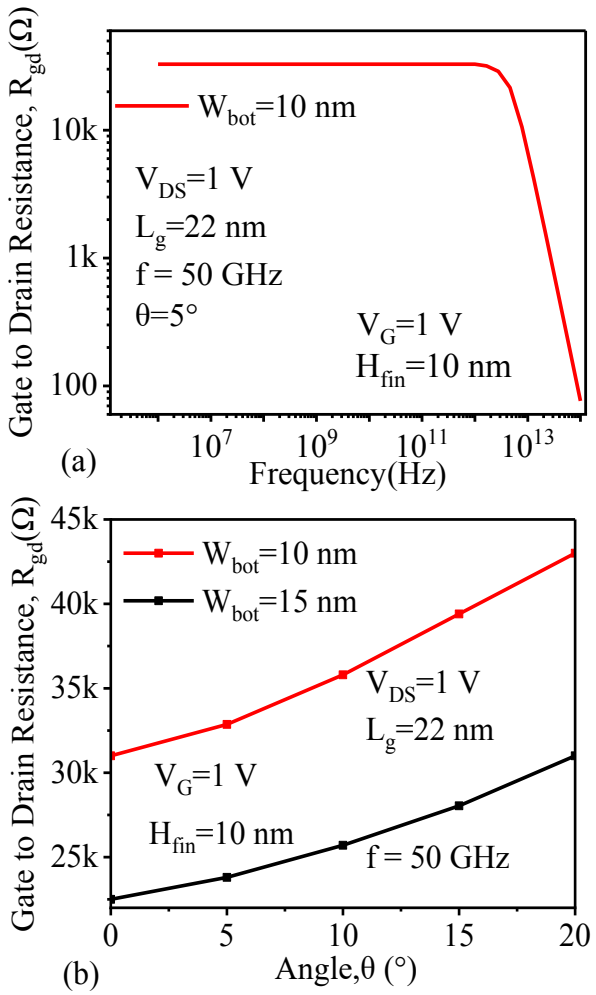

Fig. 6. Simulation results of (a) Gate to drain resistance concerning the frequency and (b) impact of inclined angles on R_{gd} for different device bottom widths.

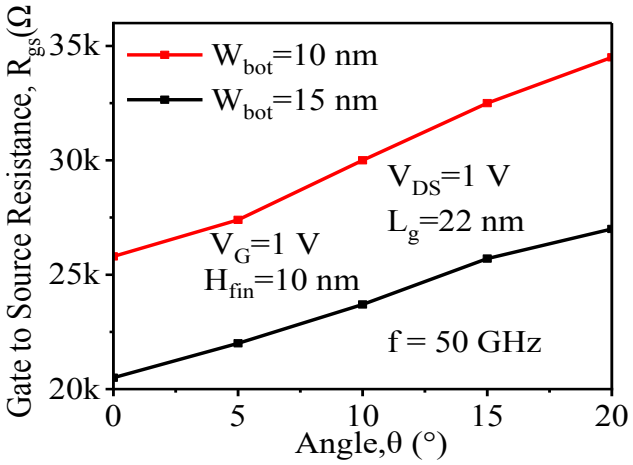

Fig. 7. Simulation results of the impact of inclined angles on Gate to Source capacitance at a frequency of 50 GHz for different device bottom widths.

Fig. 8(a) illustrates the transconductance (g_m) behavior concerning the operating frequency at W_{bot} = 10 nm, for given bias conditions V_{gs}=1 V and V_{ds}= 1 V. When the operating frequency is below the cut-off frequency, g_m remains unchanged with change in operating frequency. Fig. 8(b) demonstrates the effect of inclined sidewalls on the g_m. When the θ varies from 0° to 20° at W_{bot} = 10 nm, g_m reduces by almost 19%. Likewise, for W_{bot} = 15 nm, g_m decreases by almost 20% as θ varies from 0° to 20°. The rise in θ results in a decrease in the channel cross-section area which leads to the reduction of drain current. Thus, the g_m decreases with the

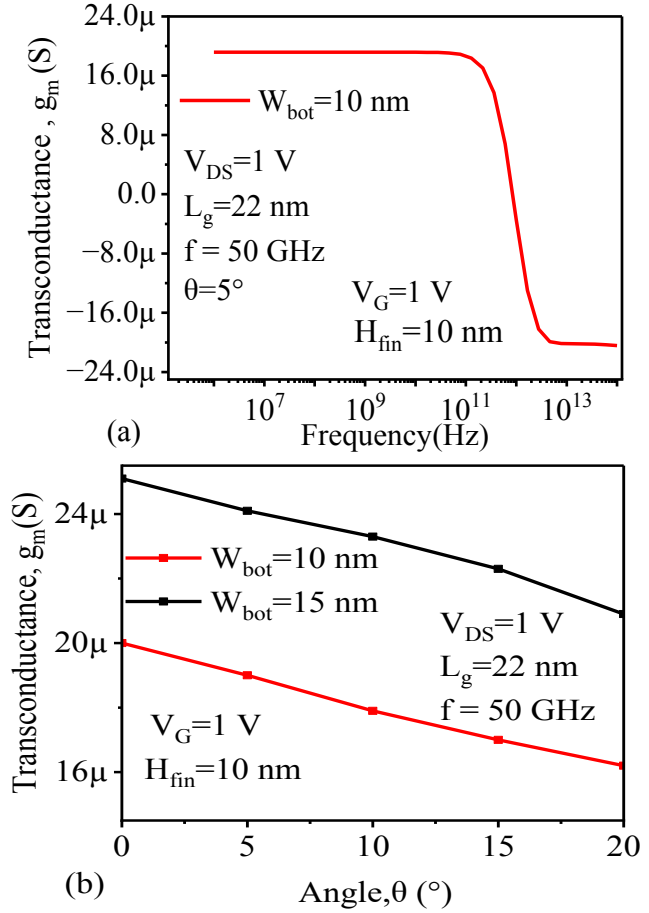

Fig. 8. Simulation results of (a) Transconductance concerning the frequency and (b) impact of inclined angles on g_m for different device bottom widths.

rise in θ. Similarly, Fig. 9 shows the impact of the inclination angle θ on gate-to-source conductance (g_{ds}). For W_{bot} = 10 nm, g_{ds} decreases by almost 34% as inclined angles θ vary from 0° to 20° whereas, at W_{bot} = 15 nm, g_{ds} decreases by almost 33% as θ varies from 0° to 20°.

Fig. 10 demonstrates the impact of inclined sidewalls on the time constant (τ) at the particular frequency of 50 MHz at V_{gs}=1 V and V_{ds}= 1 V. The τ is responsible for charging and discharging delays offered by the device at very high operating frequencies. A minute variation has been noticed in τ against the variation in θ, which can be attributed to the rise in R_{gd} and R_{gs} as well as the reduction of C_{gd} and C_{gs} simultaneously. An increment in τ by 3% when θ is varied from 0° to 20° at W_{bot} = 10 nm is observed. A similar variation at W_{bot} = 15 nm is also noticed (τ increases by 4%).

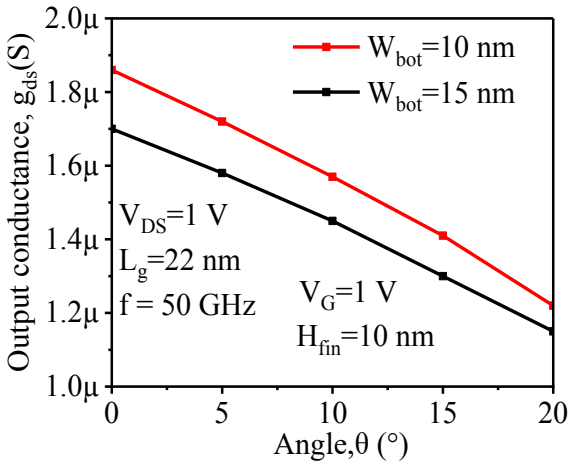

Fig. 9. Simulation results of the impact of inclined angles on the drain to source transconductance at a frequency of 50 GHz for different device bottom widths.

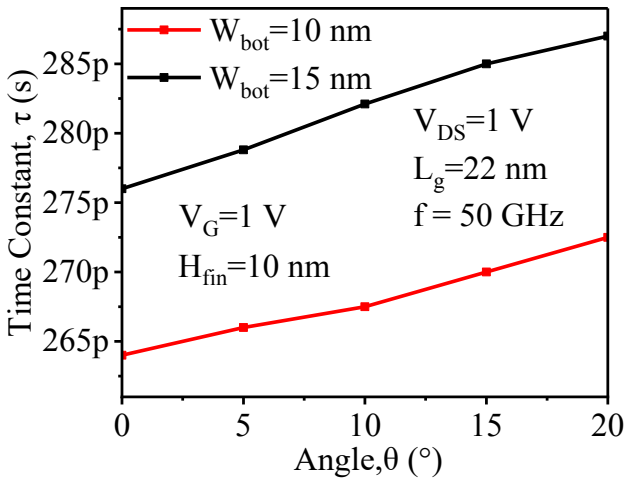

Fig. 10. Simulation results of the impact of inclined angles on time constant at a frequency of 50 GHz for different device bottom widths.

IV. Conclusion

This study thoroughly investigates the effect of process-induced inclined sidewalls on NQS small-signal parameters of NW GAA MOSFETs. To examine the small-signal parameters, calibrated simulation results have been used with the help of the 3-D TCAD Sentaurus tool. The results show that the channel distribution resistances R_{gd} and R_{gs} are the most susceptible to sidewalls angle (θ). When the inclination angle θ is increased from 0° to 20° at W_{bot} = 10 nm, R_{gd} and R_{gs} see 39% and 34% increment, respectively. Similarly, C_{gd}

and C_{gs} reduce by 14% and 16%, respectively for a similar change in θ. A minute variation in τ has been noticed with the variation in θ due to an increment in resistance and a decrease in capacitances with an increase in the inclination angle.

V. Acknowledgment

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