Hybrid Multistage Differential Rectifier for Indoor Light Energy Harvester in 65nm CMOS Technology

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***Abstract*—This paper presents a design of a hybrid multistage differential rectifier dedicated for indoor light energy harvesters. For the first stage, a fully cross- coupled rectifier with two additional PMOS switches is used and conventional fully cross-coupled rectifiers are cascaded for the succeeding six stages. The proposed rectifier is designed using TSMC 65nm CMOS process for a smaller chip area. With an input voltage of 0.5 V operating at 10 MHz, the circuit obtained an output voltage of 2.08 V and output current of 10.4 mA. It allows improving the output current to as much as twice the value compared to that of a conventional multistage differential rectifier structure. The maximum power conversion efficiency obtained is 43.08%. The total core chip area is 0.052 um^2. All the design underwent multiple thorough verifications and simulations using Synopsys Custom Design Tool.**

***Index Terms*—Internet of Things (IoT), Wireless Sensor Network, power efficiency, rectifier**

I. Introduction

Wireless Sensor Networks (WSNs) are a crucial component in the field of Internet of Things (IoT) [1]. Wireless channels combine a number of small sensors to form wireless sensor networks. [2]. The limitation of these WSNs is their limited battery life. Battery replacement and maintenance can become a hassle as they incur increased operational costs. Energy harvesting technology becomes a solution to provide batteryless operation for WSNs [3]. Solar energy harvesting is already an established technology for WSNs that are commonly used in outdoor applications [4]. This won't be suitable for indoor applications, as the luminous intensity of indoor light is not as efficient to use for photovoltaic cells as sunlight [5]. Energy harvested becomes too low under low-light conditions and will be insufficient to power up wireless sensor nodes. With this, power management circuits bridge the gap between the very low energy harvested through energy harvesting and the WSN's power dissipation [6], [7]. In an energy harvesting system, rectifiers convert AC signals to DC signals [8] - [11]. A rectifier's purpose is to convert these ambient energy such as motion, vibration and or RF which is an AC to become DC [12]. Micropower harvesters are capable of producing voltages in the range of hundreds of millivolts, necessitating the rectifier's operation with a low input voltage [13]. In line with this, rectifier needs to be operating in ultra low-power and it is a challenge to design rectifier circuits that is capable to achieve high values of PCE [14]. This PCE value is influenced by various factors which includes design topology, leakage issues, parasitic effects and threshold voltage [16]. The full gate cross-coupled topology has been widely investigated as a promising method. Compared to other topologies, this topology makes it suitable for very low power applications as only small voltage drops are carried out along its current path [8]. At low input power, a single stage rectifier doesn't have the capacity to generate sufficient DC output voltage. However, conventional multistage differential rectifiers produce a very small amount of current which is not enough to charge the rechargeable batteries used in energy harvesting systems. Therefore, this paper focuses on design and layout of a hybrid multistage differential rectifier circuit which will satisfy the specifications in indoor light energy harvesting applications.

II. CMOS Rectifier Architecture and Characteristics

A. Diode-tied Implementations

A diode-connected or diode-tied MOSFET is a specific configuration where its gate and the drain are shorted, or connected together. As seen in Figure 1, the MOSFET acts as a diode in this setup. In an NMOS transistor, this configuration results in a device that conducts current only when the V_{GS} is greater than V_{TH}, and for a PMOS transistor, the device conducts current when $|V_{GS}|$ exceeds $|V_{TH}|$. Threshold voltage V_{TH} is typically approximately 0.5 V, which is lower than that seen in conventional diodes, but it is still an important factor, especially for input voltages below a few hundred millivolts.

The performance implications of different MOSFET configurations are crucial. When a diode-connected NMOS and a diode-connected PMOS are arranged in parallel, there is reduction in total voltage drop, leading to an enhancement in PCE. Conversely, when these MOSFETs are arranged in series, its effective V_{TH} is effectively doubled, leading to a decrease in PCE [9].

B. Diode-tied Implementations Topologies

Traditional full-wave bridge rectifiers utilize four switches to generate two paths of conduction, transforming an AC input into a DC output. Two switches are working at a time in the path of conduction reducing the usable input voltage range due to the voltage drop across them. The gate cross-coupled connection shown in Figure 2(b) is used to increase the functional input range. This is achieved by decreasing the V_{TH} drop of a single switch in the path from V_{TH} to the voltage drop across the switch during forward conduction. This technique increases the PCE through the gates cross-connection, resulting in a voltage swing exceeding the diode-tied connections, subsequently boosting the overall forward current. Nonetheless, one V_{TH} drop is still incurred in the

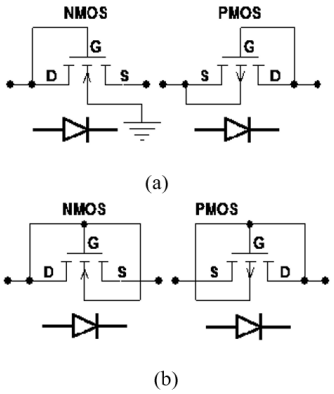

Fig. 1. Diode-tied Configurations: (a) Standard MOS Diodes, and (b) MOS Diodes with bulk and drain shorted [8]

conduction path by the remaining pair of non-gate cross-coupled switches. Fully cross-coupled full-wave rectifiers as shown in Figure 2(c), reduce the V_{TH} drops in all diodes on the current path [12].

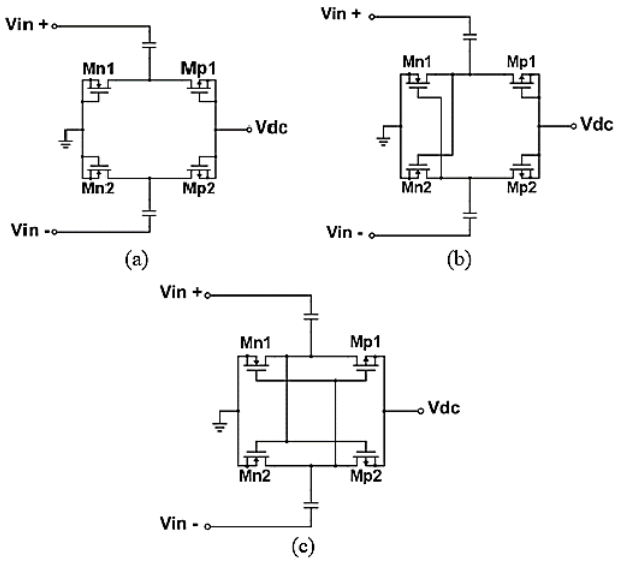

Fig. 2. CMOS Full-wave bridge rectifiers: (a) Conventional Topology, (b) Gate Cross-Coupled Topology, (c) Fully Cross-Coupled Topology [12]

C. Differential Self-V_{TH}-Cancellation Rectifier

The Negative Voltage Converter (NVC) or differential self-V_{TH}-cancellation rectifier (DSVC) circuit in Figure 3 allows only a small voltage drops in its path inherent to its full gate cross coupled topology.

During the positive interval from the input, when input is less than V_{TH}, transistors (M_{P1}, M_{N2}) are off therefore, no current flows to the load. As input voltage increases more than V_{TH}, both transistors (M_{P1}, M_{N2}) are turned on. During the negative interval of input, operation is similar with the positive interval but with the other two transistors (M_{P2}, M_{N1}) in operation.

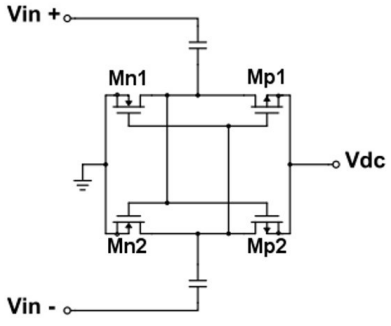

Fig. 3. A Single-Stage Differential Self-VTH -Cancellation Rectifier [12]

III. Conventional Differential Rectifier and Two-Stage Voltage Multiplier Circuit

A. Conventional Two-Stage Differential-Drive Rectifier Circuit

Shown in Figure 4 is the conventional two-stage differential-drive rectifier. The two stages function as voltage doublers (V_{D1} and V_{D2}). The two paths work alternately depending on input amplitude looking at the common-gate terminal. One side will be in forward conduction mode or the charging phase and the other side will be in reverse conduction mode or the discharging phase. During each cycle, the roles are reversed for the two sides.

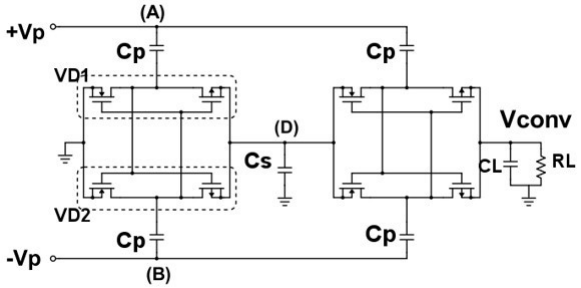

Fig. 4. Conventional two-stage differential-drive rectifier circuit [18]

Considering the voltage doubler (V_{D1}) in Figure 4, Kirchoff's Voltage Law can be used to obtain the voltage across C_P during the charging phase given by,

$$V_{cp} = -V_p + V_{dn} \tag{1}$$

Considering the capacitors as ideal, during discharging phase, the charge stored in C_P is transferred to storage capacitor C_S. Thus, the voltage across C_S will yield,

$$V_{dc} = 2V_p - (V_{dn} + V_{dp}) \tag{2}$$

When a second stage is cascaded, the voltage (V_{dc}) will function as the DC source for it. Voltage on the fly-capacitor C_P on the second-stage becomes,

$$V_{dc} = -3V_p - (V_{dn} + V_{dp}) \tag{3}$$

Following the discharging phase in the second stage, rectified DC voltage V_{conv} delivered to the load will be,

$$V_{dc} = 4V_p - 2(V_{dn} + V_{dp}) \tag{4}$$

Through recursion analysis, general equation of output DC voltage for N-stages becomes,

$$V_{conv} = 2N * V_p - N * (V_{dn} + V_{dp}) \quad (5)$$

As seen in (5), increase in voltage loss because of the threshold voltage is directly proportional with the increase in number of stages.

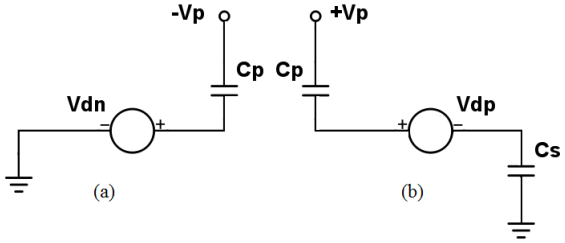

Fig. 5. Equivalent circuit of voltage doubler when in: (a) charging phase and (b) discharging phase [18]

B. Two-Stage Voltage Multiplier Circuit

From the assumption of relation of threshold voltage with number of stages, the study in [18] stated that input signal amplitude must exceed threshold voltage. To overcome this, auxiliary voltage source can be added so that,

$$V_{out} = N(2V_{in} - V_{drop}) + V_{aux} \quad (6)$$

The implementation of auxiliary voltage is at the gate of these rectifying transistors so that these transistors will operate in either linear or saturation region thereby improving rectifier performance. Similar works are done that use biasing the gate-terminal of transistors in [19] and [20]. The circuit shown on Figure 6 is a two stage voltage multiplier consisting of a differential drive rectifier cascaded with the PMOS switches (P1, P2). These PMOS switches are gate-cross-coupled. The first stage will generate the bias input signal and this signal appearing on the gate of these switches. According to [18], increasing the number of stages won't be beneficial. This is further explained in [20].

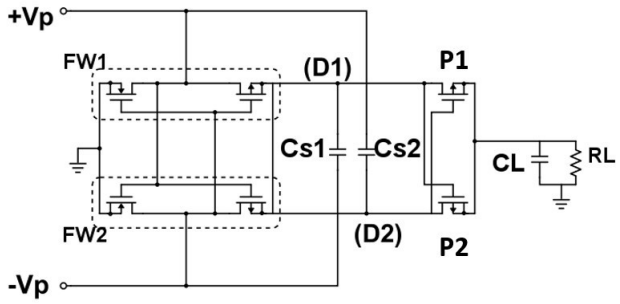

Fig. 6. Schematic of two-stage voltage multiplier [18]

IV. Proposed Hybrid Multistage Differential Rectifier

Some applications might need higher DC voltage. By employing multistage configuration, as shown in Figure 8, in theory, it acts as a voltage multiplier.

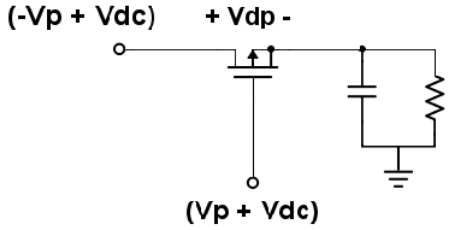

Fig. 7. Schematic of gate-cross-coupled switch [18]

The two-stage voltage multiplier circuit architecture proposed in [18] will serve as the first stage of the design due to its high output current due to minimal reverse leakage resulting from the high gate voltage. Its architecture employs a straightforward method to DC bias input signal before delivering to subsequent stages. Conventional two-stage differential-drive rectifiers are then used in the succeeding N stages. Smoothing capacitors (C_s) are inserted in between stage minimizing the ripples in the output stage.

V. Simulation Results

A. Conventional vs Proposed

Figure 9 and 10 shows the output voltage and output current of conventional multistage rectifier and the proposed multistage rectifier at different loads with uniform parameters. Both architectures operate at an input voltage of 0.5V at 10 MHz frequency.

Based from simulation results, proposed design generated greater output DC voltage and current compared to the conventional multistage rectifier at different loads.

B. Pre-Simulation vs Post-Simulation

The proposed hybrid multistage rectifier is designed to have 2V output voltage with current greater than the battery's trickle current (>6mA). Figure 11 shows that the FF and SS corners exhibit a significant difference in voltage (V_{FF} = 2.15V, V_{SS} = 2.09V) and current (I_{FF} = 10.4mA, I_{SS} = 10.5mA) compared to the TT corner but are still in tolerable range. Although such is the case, the pre-simulation results show that the proposed hybrid multistage rectifier still met the target specifications at an input of 0.5 V and a load of 200Ω for different corners.

Figure 12 shows post-layout simulation results for the proposed hybrid multistage rectifier at different corners. The FF and SS corner exhibits a very slight difference from the TT corner in its output values (V_{FF} = 2.04V, I_{FF}= 10.2mA) and (V_{SS} = 2.07V, I_{SS} = 10.4mA). Variation of post-layout from pre-layout simulation results is an effect of parasitic capacitances that arise due to the layout techniques used.

C. Power Conversion Efficiency at Different Load Current

Power conversion efficiency (PCE) is stated as the relationship between the absorbed power and the load power. It is the main parameter in performance evaluation of a rectifier.

A high PCE signifies high efficiency, however, in practical applications, nonlinear losses V_{th} loss and leakage currents are unavoidable. Figure 13 shows the PCE of proposed hybrid multistage rectifier circuit at increasing load.

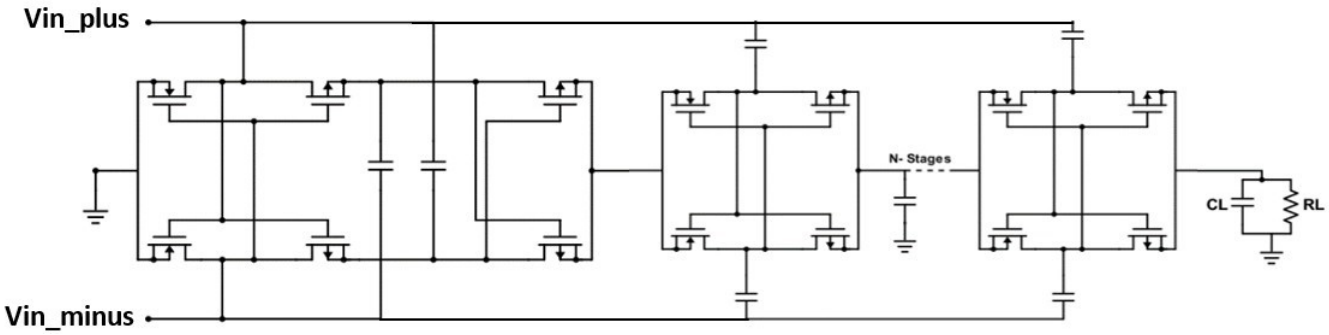

Fig. 8. Schematic of proposed hybrid multistage differential rectifier

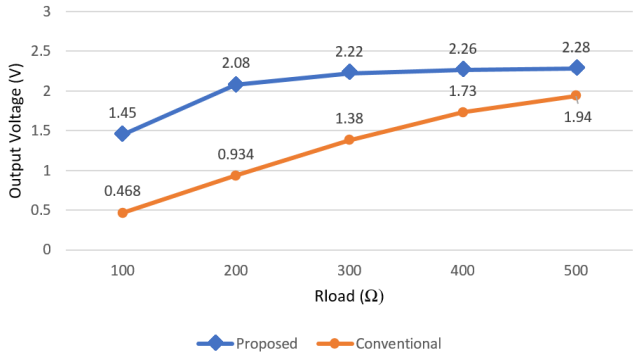

Fig. 9. Output voltage for proposed and conventional rectifier at different loads.

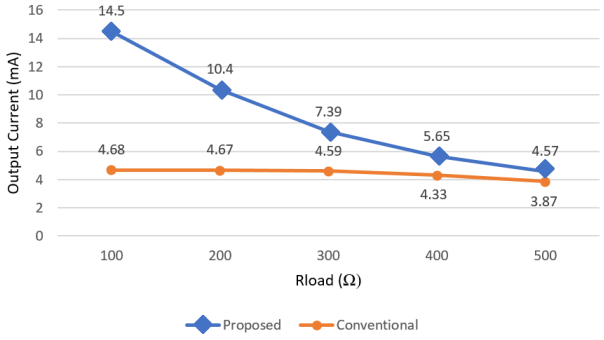

Fig. 10. Output current for proposed and conventional rectifier at different loads.

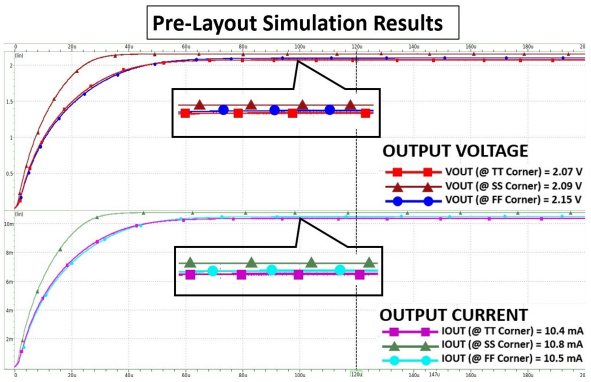

Fig. 11. Pre-layout simulation results of the proposed hybrid multistage rectifier at various corners.

Table 1 shows the PCE of proposed hybrid multistage

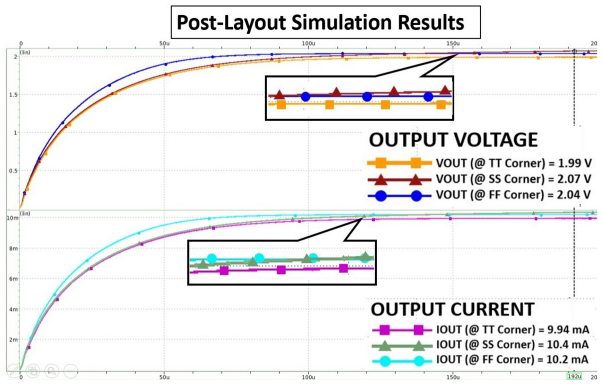

Fig. 12. Post-layout simulation results of the proposed hybrid multistage rectifier at various corners

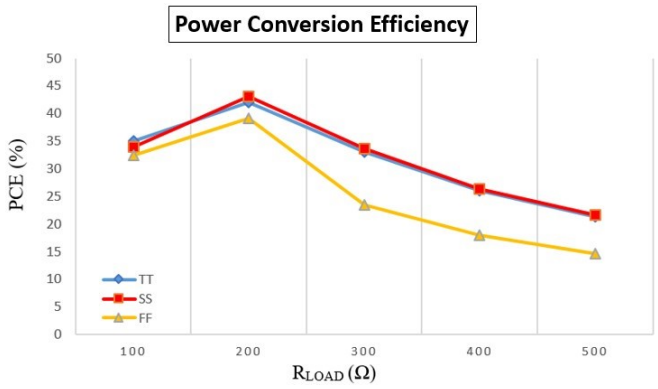

Fig. 13. PCE vs load resistance for the designed rectifier.

rectifier circuit at different current loads. Analyses were made at all corners. Maximum efficiency of 43.08% is achieved. The data in Table 1 was obtained using the equation,

$$PCE = \frac{V_{dc} * I_{dc}}{\frac{1}{T}\int_{t1}^{t1+T} V_{RFin}(t) * I_{in}(t)dt} \tag{7}$$

D. Chip Layout

The top-level layout is shown in Figure 14, which is a combination of the seven stages. The dimension of the chip is 279.43 um x 186.26 um. Hence, the total chip core design area is 0.052 um^2.

A clearer view of the first and second stages are shown in Figure 15 and Figure 16, respectively. The layout shown in Figure 16 is also used for the remaining stages.

TABLE I
PCE OF PROPOSED HYBRID MULTISTAGE RECTIFIER AT DIFFERENT LOAD CURRENT FOR ALL CORNERS.

Process Corner	14.5mA	10.4mA	7.39mA	5.65mA	4.57mA
TT	34.99%	42.02%	32.98%	26.08%	21.33%
SS	34%	43.08%	33.64%	26.42%	21.64%
FF	32.38%	39.09%	23.51%	18.03%	14.6%

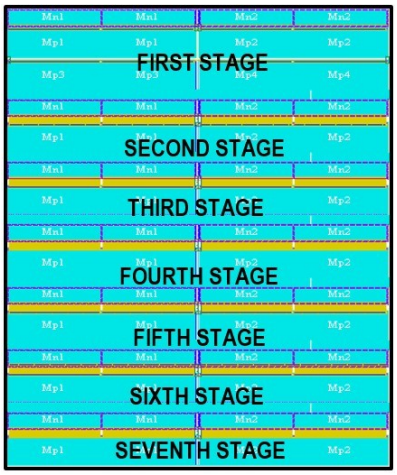

Fig. 14. Chip layout of the proposed hybrid multistage rectifier.

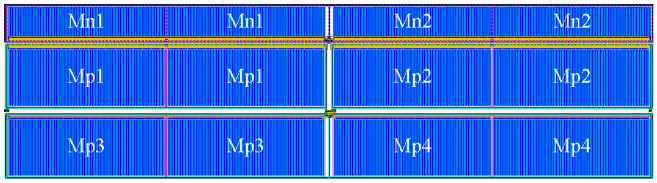

Fig. 15. First Stage Layout

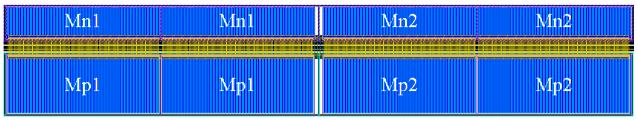

Fig. 16. Second Stage Layout

E. Comparison to Similar Works

Table 2 shows the performance comparison of the proposed design and to other published works. In the proposed design, the high output current performance can be advantageous in some applications that requires high current.

VI. CONCLUSION

A hybrid multistage differential rectifier circuit has been designed in TSMC 65nm 1P9M process. The system uses two architectures: a two-stage voltage multiplier circuit with PMOS switches as the first stage and cascaded single-stage fully cross-coupled rectifiers for the succeeding stages. Smoothing capacitor is added in between stages to minimize output ripple. The design improved the voltage extraction and obtain a higher output current to power the load and the battery that constantly supplies a load.

The circuit has been designed in 7 stages with a DC input voltage of 0.5 V extracted from a single photovoltaic cell. The design proved to achieve the target specifications for the load and the NiMH rechargeable battery at lower input voltage. The circuit obtained a decent performance with a voltage output of 2.08 V and current output of 10.4mA. The maximum power conversion efficiency obtained is 43.08%. The total core chip area is 0.052 um^2.

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TABLE II
PERFORMANCE COMPARISON

Reference	**This Work**	**[15]**	**[17]**	**[21]**
CMOS Technology	**65 nm**	180 nm	180 nm	90 nm
Input Voltage	**0.5 V**	0.5 V	0.5 V	0.5 V
Output Voltage	**1.99 V**	1.3 V	1.3 V	1.39 V
Output Current	**9.94 mA**	204 μA	100 μA	50 - 300 μA
Operating Frequency	**10 MHz**	-	-	27 MHz
Number of Stages	**7**	3	2	3
Chip Area	**0.052 μm^2**	-	-	-
Conversion Principle	**Differential-Drive Multistage Rectifier**	Differential-Drive Multistage Rectifier	Differential-Drive DTCMOS Charge Pump	Differential-Drive Multistage Rectifier

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