Grounded Series/Parallel RC Impedance Simulators with a Single VDBA

Pitchayanin Moonmuang, Tattaya Pukkalanun, Masaaki Fukuhara, and Worapong Tangsrirat

***Abstract*— This article presents grounded RC series/parallel impedance simulator circuits employing a single voltage differencing buffered amplifier (VDBA) as an active element. The proposed RC series impedance simulator consists of one capacitor and one resistor, while the proposed grounded RC parallel type requires only a single capacitor as a passive element. The simulated equivalent resistance and capacitance values can be tuned electronically through the transconductance gain of VDBA device which can be adjusted by means of the external biasing current. The performance validation of the proposed circuits including the resonant circuit application is proved by simulation results via PSPICE software based on TSMC 0.25-μm CMOS technology.**

I. Introduction

Designing integrated circuits is a continuously evolving technology that has considerably reduced in size but maintained high performance. To fulfill the rapid growth of designing various types of analog signal processing circuits, active devices have been known. Active devices provide the following advantages: Their physical characteristics are small, so they occupy less space in the integrated circuit and have a wide operational frequency range. The VDBA [1], or active device, which was recently proposed, has an uncomplicated design that makes it widely applicable, such as a filter circuit [2], inductance simulator [3], and capacitance multiplier [4]. A review of the research [4] noticed that the proposed circuit's performance was slightly different from the theoretical result. Since the actual equivalent capacitance includes unwanted impedance, energy loss occurs in the circuit. As a result, an RC impedance simulation circuit that is capable of adjusting the equivalent capacitance and equivalent resistance was created, which could decrease the dissipated power in the circuit, as illustrated by the research presented in [5]. However, the circuit shown in [5] requires two active and three passive components to be synthesized, which takes up a lot of chip area and is unable to be modified electrically.

The article proposes grounded RC series/parallel impedance simulator circuits that can electronically adapt the equivalent capacitance and equivalent resistance by altering the external bias current. The presented two circuits were constructed up of one VDBA circuit and one capacitor, which in an RC series configuration are essential to connect with a single resistor and without additional resistors in an RC parallel configuration. The proposed circuit's simulated results were given using the PSPICE program and TSMC's 0.25 μm CMOS technology, including its applicability in resonant circuits.

II. VDBA's Circuit Description

The schematic symbol in Fig. 1 shows details of the VDBA device which has two input ports (p, n) and two output ports (z, w). An ideal qualification of the VDBA can be given in (1). The differential voltage between v_p and v_n ($v_p - v_n$) is converted by the transconductance g_m into a current i_z at the terminal z. The voltage drop at the z terminal (v_z) is then converted to the output voltage v_w at the terminal w.

$$\begin{bmatrix} i_p \\ i_n \\ i_z \\ v_w \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ g_m & -g_m & 0 & 0 \\ 0 & 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} v_p \\ v_n \\ v_z \\ i_w \end{bmatrix} \tag{1}$$

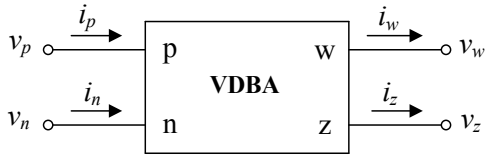

Figure 1. Schematic symbol of the VDBA.

The g_m is the small signal transconductance gain of the VDBA. The value of g_m is electronically controllable by a bias current that can be electronically controlled, which is a tool for designing the proposed circuit. For non-ideal VDBA, the defined equation becomes:

$$\begin{bmatrix} i_p \\ i_n \\ i_z \\ v_w \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ \alpha g_m & -\alpha g_m & 0 & 0 \\ 0 & 0 & \beta & 0 \end{bmatrix} \begin{bmatrix} v_p \\ v_n \\ v_z \\ i_w \end{bmatrix}, \tag{2}$$

In above relation, $\alpha = (1 - \varepsilon_{gm})$ and $\beta = (1 - \varepsilon_v)$, where $|\varepsilon_{gm}| << 1$ denotes the transconductance inaccuracy, and $|\varepsilon_v| << 1$ represents the voltage tracking coefficients.

The structural circuit of VDBA device has been designed by CMOS technology with TSMC 0.25-μm as shown in Fig. 2 [6]. It consists of two circuits, namely the transconductor circuit (M_1-M_4) and the voltage buffer circuit (M_5-M_9). The characteristic equation of g_m can be given as follows:

$$g_m = \sqrt{\mu C_{ox} \left(\frac{W}{L}\right) I_B}, \tag{3}$$

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where μ is the effective carrier mobility, C_{ox} is the gate-oxide capacitance per unit area, and W and L are the effective channel width and length, respectively. The adjustable biasing current in Fig. 2 can also be used to control electrically the proposed VDBA device.

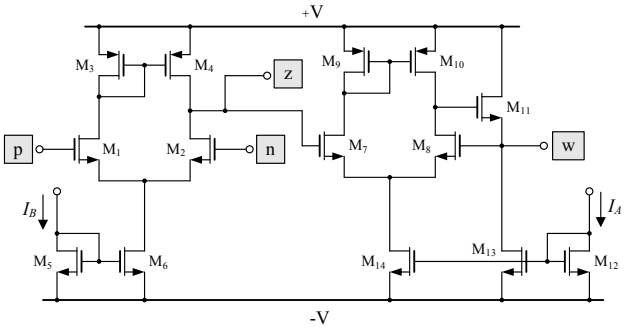


Figure 2. CMOS structure of the VDBA.

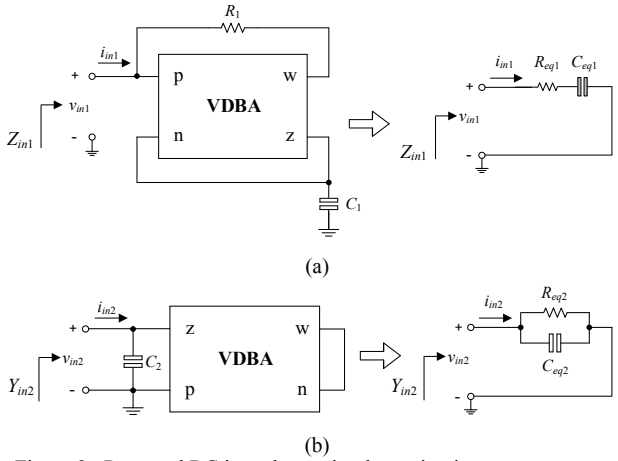
III. Proposed RC Impedance Simulator Circuits

The proposed circuits seen in Fig. 3 are grounded RC impedance simulators with series and parallel types. Considering the VDBA's ideal operation, the input impedance (Z_{in1}) for Fig. 3(a) and input admittance (Y_{in2}) for Fig. 3(b) can be expressed as, respectively,

$$Z_{in1} = \frac{v_{in1}}{i_{in1}} = R_{eq1} + \frac{1}{sC_{eq1}} = R_1 + \frac{R_1 g_m}{sC_1} \quad , \tag{4}$$

and

$$Y_{in2} = \frac{i_{in2}}{v_{in2}} = \frac{1}{R_{eq2}} + sC_{eq2} = g_m + sC_2 \quad . \tag{5}$$



(a)

(b)

Figure 3. Proposed RC impedance simulator circuits.
(a) series type (b) parallel type

The simulated equivalent resistance (R_{eq}) and equivalent capacitance (C_{eq}) of the proposed circuits can be expressed as follows:

For Fig. 3(a) $$R_{eq1} = R_1 \quad \text{and} \quad C_{eq1} = \frac{C_1}{R_1 g_m}, \tag{6}$$

For Fig. 3(b) $$R_{eq2} = \frac{1}{g_m} \quad \text{and} \quad C_{eq2} = C_2 . \tag{7}$$

For a series type in (6), the first step is to adjust R_{eq1} in terms of R_1. After that, the C_{eq1} can be electronically tuned using the g_m of VDBA device. Moreover, the R_{eq2} and C_{eq2} of a parallel type in (7) can be controlled separately from each other.

In the non-ideal condition, the terminal relationship of voltage and current can be defined as: $i_p = i_n = 0$, $i_z = \alpha g_m(v_p - v_n)$, and $v_w = \beta v_z$, where the α provided transconductance tracking error and β gives the non-ideal voltage gain. If the non-ideal equation of VDBA is considered, the input impedance and input admittance of both proposed circuits become:

For Fig. 3(a); $$Z'_{in1} = R'_{eq1} + \frac{1}{sC'_{eq1}} + R_{extra1} + sL_{extra1} \tag{8}$$

where $$R'_{eq1} = R_1 \quad , \quad C'_{eq1} = \frac{C_1}{\alpha R_1 g_m} \tag{9}$$

and $$R_{extra1} = \frac{R_1}{1-\beta} \quad , \quad L_{extra1} = \frac{R_1 C_1}{\alpha g_m (1-\beta)} \quad . \tag{10}$$

For Fig. 3(b); $$Y_{in2} = \frac{1}{R'_{eq2}} + sC'_{eq2} \quad , \tag{11}$$

where $$R'_{eq2} = \frac{1}{\alpha\beta g_m} \quad \text{and} \quad C'_{eq2} = C_2 . \tag{12}$$

The impact of a specific passive and active variable R_1, C_1, C_2, g_m R_{ex}, α, and β on the following sensitivity outcomes R'_{eq}, C'_{eq}, R_{ex}, and L_{ex}:

For Fig. 3(a); $$S_{R_1}^{R'_{eq}} = S_{C_1}^{C'_{eq}} = -S_{R_1}^{C'_{eq}} = -S_{g_m}^{C'_{eq}} = -S_{\alpha}^{C'_{eq}} = 1, \tag{13}$$

$$S_{\beta}^{R_{extra}} = \beta/(1-\beta) < 1 \, , \; S_{R_1}^{R_{extra}} = 1 \, , \tag{14}$$

$$S_{R_1}^{L_{extra}} = S_{C_1}^{L_{extra}} = -S_{\alpha}^{L_{extra}} = -S_{g_m}^{L_{extra}} = 1 \, , \tag{15}$$

and $$S_{\beta}^{L_{extra}} = \beta/(1-\beta) < 1 \tag{16}$$

For Fig. 3(b); $$S_{g_m}^{R'_{eq}} = S_{\alpha}^{R'_{eq}} = S_{\beta}^{R'_{eq}} = -S_{C_2}^{C'_{eq}} = -1 \tag{17}$$

The investigation explores sensitivity outcomes at the proposed RC impedance simulators and discovers that the performance is less than one in magnitude.

IV. Simulation Results

This article expands on the characteristics in order to demonstrate the simulation result of the RC impedance simulator using PSPICE, where the VDBA element used in these simulations was designed with TSMC's 0.25 μm technology model parameters. The present section expands on the features to demonstrate the simulation result of the RC impedance simulator employing PSPICE program. The dimensions W/L (μm/μm) of all transistors were chosen as: 25/0.25 for M_1-M_2, M_5, M_7-M_8, and M_{12}. whereas 35/0.25 were selected for M_3-M_4, M_9-M_{10}, and M_{13}-M_{14}. The other transistors, M_6 and M_{11} are equal to 30/0.25. The working supply voltages (±V) were set to be 0.75V.

The proposed circuit appears in Fig. 3(a), and the frequency responses in magnitude and phase angle of a grounded RC series impedance simulator are given in Fig. 4. The chosen values of elements are v_{in} = 50 mV (peak), R_1 = 1 kΩ, C_1 = 1 nF and I_B = 100 μA ($g_m \cong$ 1.58 mA/V), which results in R_{eq} = 1kΩ and C_{eq} = 0.632 nF. To simulate the time-varying response in Fig. 5, the phase angle i_{in} leading v_{in} is 48.60° at f = 100 kHz, which is nearly to the theoretical result of 51.55° with a maximum error of 5.72%. The amplitude and phase versus frequency responses of the grounded RC parallel impedance simulator in Fig. 3(b) with C_2 = 1 nF are shown in Fig. 6, which provide the findings R_{eq} = 632Ω and C_{eq} = 1 nF from (6). The phase angle i_{in} leading v_{in} is 60.48° at f = 400 kHz for simulating the time-varying response shown in Fig. 7, which is close to the theoretical result of 57.86° with a maximum error of 4.53%. The simulations report that the operation of proposed circuits are consistent and follow theoretical concepts.

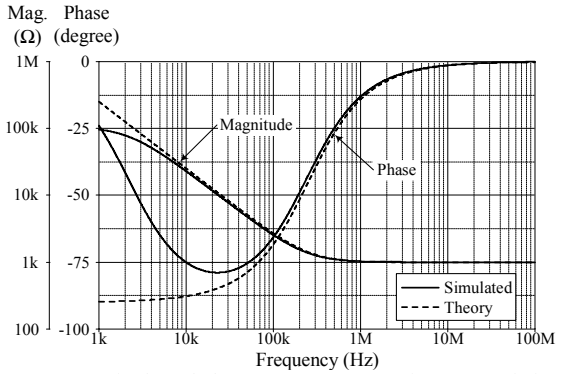


Figure 4. Magnitude and phase responses versus frequency of Fig. 3(a).

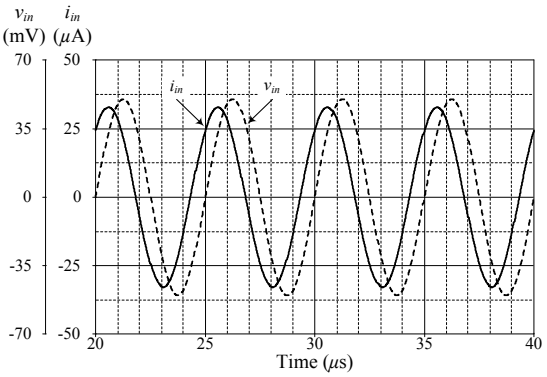


Figure 5. Phase difference between i_{in} and v_{in} versus time of Fig. 3(a).

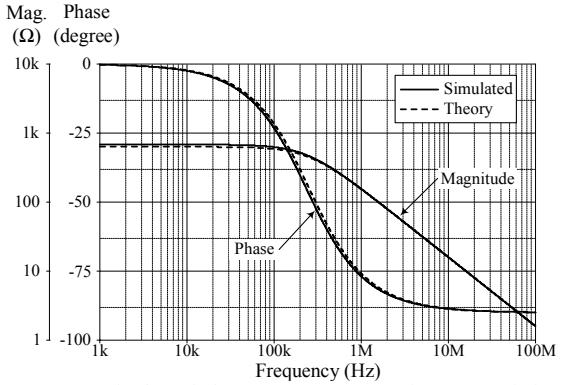


Figure 6. Magnitude and phase responses versus frequency of Fig. 3(b).

Figs. 8 and 9 respectively depict the impedance magnitude (Z_{in}) versus frequency responses of a grounded RC impedance simulators in Figs.3(a) and 3(b), whose equivalent resistances and capacitances obtained as shown in Table 1 from a following set of components: R_1 = 1 kΩ and C_1 = C_2 = 1 nF, with varying bias current I_B = 120 μA ($g_m \cong$ 1.58 mA/V), 250 μA ($g_m \cong$ 2.5 mA/V) and 500 μA ($g_m \cong$ 3.54 mA/V), respectively. The power dissipated in the proposed circuits, which are grounded RC impedance simulators with series and parallel types, is equal to 0.38 mW.

TABLE I. VALUES OF R_{EQ}, C_{EQ} AND Z_{IN} AS A FUNCTION OF I_B

Proposed circuits	I_B (μA)	R_{eq} (Ω)	C_{eq} (nF)	Z_{in} (Ω) at f = 100 kHz	
				Theoretical	Simulation
Fig. 3(a)	120	1k	0.58	2.74k	2.93k
	250		0.40	3.96k	4.10k
	500		0.28	5.18k	5.71k
Fig. 3(b)	120	577	1	585.05	542.45
	250	400		403.78	387.94
	500	283		303.37	278.63

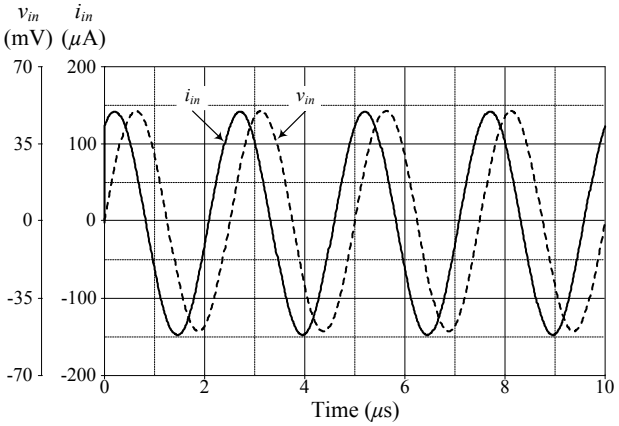


Figure 7. Phase difference between i_{in} and v_{in} versus time of Fig. 3(b).

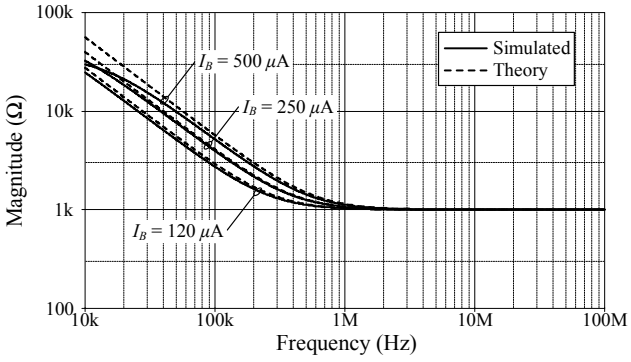


Figure 8. Magnitude Z_{in} versus frequency of Fig. 3(a) when varying I_B.

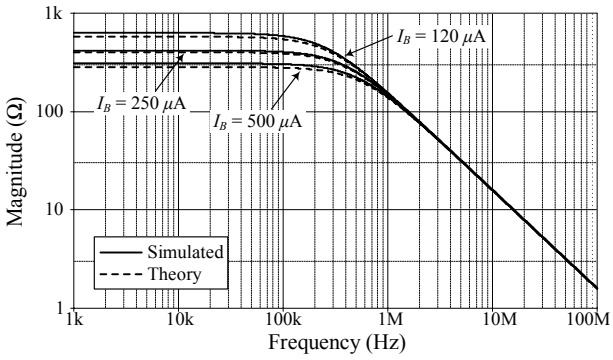


Figure 9. Magnitude Z_{in} versus frequency of Fig. 3(b) when varying I_B.

V. APPLICATION

A resonant circuit application is shown in Fig. 10 based on the use of the proposed ground RC series simulator in Figure 3(a). The circuit components are taken as: v_{in} = 50 mV (peak), L = 1 mH, R_1 = 1 kΩ and C_1 = 1 nF, while the bias current is varied to 100 μA 250 μA and 500 μA. The equivalent values of R_{eq} equal to 1kΩ and C_{eq} equal to 0.632 nF, 0.4 nF, and 0.26 nF, respectively, are obtained in this setting. Fig. 11 depicts the frequency responses in amplitude and phase angle of a resonant circuit using the proposed RC series simulator.

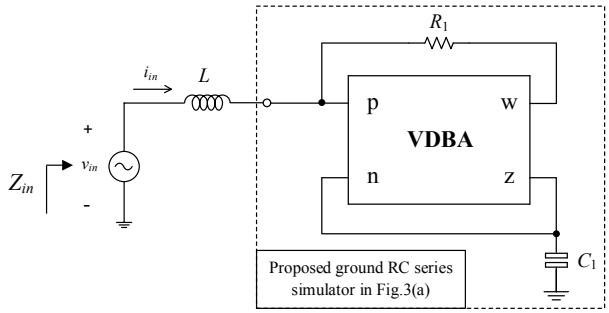


Figure 10. Resonant circuit realized with the proposed RC simulator in Fig.3(a).

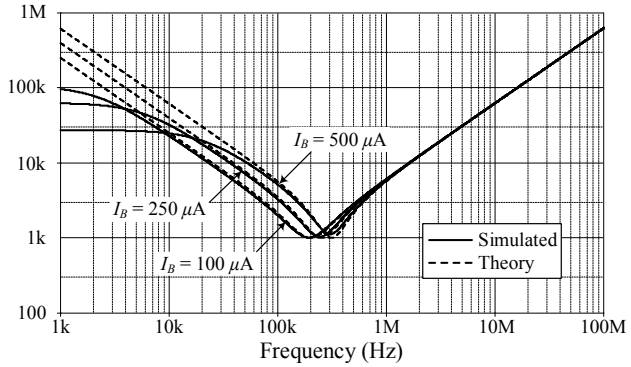


Figure 11. Frequency responses of resonant circuit in Fig. 10.

VI. CONCLUSIONS

This paper presents a series/parallel ground RC impedance simulator using a single VDBA device. For RC series-type designs with one capacitor and one resistor. while, in an RC parallel-type setup, by one capacitor and not adding the external resistor, the equivalent resistance and capacitance can be electronically modified by adjusting the bias current externally to the circuit. For the operation of the proposed circuit, TSMC's 0.25-μm CMOS technology was used to simulate characteristic results and applications in resonant circuits, utilizing the PSPICE tool to demonstrate the proposed circuit's operation.

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