A Layout Area Reduction of Basic Logic Element by Using a Neuron CMOS Type 4-input Variable Logic Circuit

Shoma Ito
Graduate School of Information and Telecommunication Engineering
Tokai University
Tokyo, Japan
2cjnm021@mail.u-tokai.ac.jp

Hisaya Sawada
Graduate School of Information and Telecommunication Engineering
Tokai University
Tokyo, Japan
3cjnm013@mail.u-tokai.ac.jp

Hirotaka Furukawa
Department of Embedded Technology, School of Information Telecommunication Engineering
Tokai University
Tokyo, Japan
0cjk1201@mail.u-tokai.ac.jp

Naruaki Hokari
Department of Embedded Technology, School of Information Telecommunication Engineering
Tokai University
Tokyo, Japan
0cjk1206@mail.u-tokai.ac.jp

Daishi Nishiguchi
Research Institute of Science and Technology
Tokai University
Kumamoto, Japan
daishi@tsc.u-tokai.ac.jp

Masaaki Fukuhara
Graduate School of Information and Telecommunication Engineering
Tokai University
Tokyo, Japan
fukuhara@tokai.ac.jp

***Abstract*—As Field Programmable Gate Arrays (FPGAs) become large integration, the area reduction of a Basic Logic Element (BLE), which is a circuit for a logical definition in FPGAs, is required. We have studied a Variable Logic Circuit (vVLC) using neuron CMOS inverters (vCMOSs) and have proposed a 4-input Variable Logic Circuit (4-vVLC) as an alternative circuit against a 4-input Look-Up Table circuit (4-LUT) in the ordinary BLE. In this paper, we describe the 4-vVLC configuration and operations, and verify that the results of the HSPICE simulations and the theoretical performances are in general agreement. In addition, we design a layout of BLEs using 4-vVLC to reduce the BLE area and compare the 4-LUT and 4-vVLC.**

Keywords—Neuron CMOS inverter, Variable Logic Circuit, FPGA, LUT, HSPICE simulation, layout area

I. Introduction

Programmable integrated circuits (ICs) have been developing in recent years, and Field Programmable Gate Arrays (FPGAs) are a prime example. The logic functions of the FPGA can be changed without hardware modification after manufacturing. Fig. 1 shows the overview of a traditional FPGA [1], which consists of three main elements: logic elements (logic blocks), input/output elements (input/output blocks), and routing elements (switch block, connection block, and routing channel). A circuit called BLE (Basic Logic Element), which is the fundamental element of logic blocks, includes a Look-Up Table (LUT) circuit. As the number of integrated BLEs in an FPGA increases, the constraints of the chip area for the logic block have become an issue. To solve the issue, we have studied a neuron CMOS type Variable Logic Circuit (vVLC), where the neuron CMOS operates intelligently like a biological neuron [2, 3, 4]. The vVLC performs some variable logic functions required as FPGA logic elements, and a 4-input Variable Logic Circuit (4-vVLC) has been proposed in ref. [5]. A 4-input LUT (4-LUT) in the BLE requires sixteen memory cells to achieve sixteen logic functions, whereas 4-vVLC requires three memory cells to perform eight logic functions. Therefore, the BLE area could be reduced by using 4-vVLC instead of the 4-LUT, although the logic functions are limited.

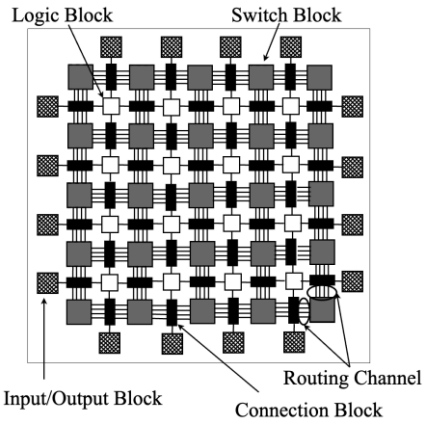


Fig. 1. Overview of traditional (island-style) FPGA

In this paper, we describe the circuit configuration and operations of the proposed 4-vVLC and verify that the waveforms of the HSPICE simulations and the theoretical results with the Floating-Gate Potential Diagram (FPD) are in general agreement. In addition, we design the layout of BLEs using 4-vVLC by Rohm 0.18μm design rules to reduce the BLE area and compare the 4-LUT and 4-vVLC.

This paper has been divided into five parts. Section Two explains the configuration and operation of the proposed circuit, Section Three evaluates the area, and Section Four discusses the evaluation results. Finally, Section Five is the conclusion.

II. Circuit Configuration and Operations

A. Neuron CMOS inverter

The 4-vVLC has neuron CMOS inverters (vCMOSs) that use Neuron MOSFETs (vMOSs) [6]. The vMOS is an electronic device with multiple capacitively coupled inputs to

the gate of a MOSFET. Fig. 2(a) illustrates the circuit diagram of the νCMOS, and Fig. 2(b) shows the circuit symbol of the νCMOS. V_1 to V_n are input signals, and C_1 to C_n are electrical capacitances between the input terminals and the floating gate (FG). The νCMOS has the gate capacitances of nMOS and pMOS in common and is connected complementarily similarly to an ordinary CMOS inverter. Assuming that the capacitance between the substrate and FG is negligible and that the initial charge of FG is 0[C], V_{FG} is expressed as

$$V_{FG} = \frac{\sum_{i=1}^{n} C_i V_i}{C_T}, \tag{1}$$

where

$$C_T = \sum_{i=1}^{n} C_i. \tag{2}$$

The output voltage V_{OUT} of νCMOS is determined by the relationship between the threshold inversion voltage V_{INV} of νCMOS and the FG voltage V_{FG}, and is expressed by the following equation.

$$V_{OUT} = \begin{cases} V_{DD} \; if \; V_{FG} < V_{INV} \\ 0 \; if \; V_{FG} > V_{INV} \end{cases} \tag{3}$$

However, the FG of νCMOS is not connected anywhere in the circuit. Therefore, there is a possibility of malfunction due to the influence of the initial charge at the time of chip manufacturing.

B. 4-input Variable Logic Circuit

The 4-νVLC, as illustrated in Fig. 3, has four input signals (V_{inA}, V_{inB}, V_{inC}, and V_{inD}), three control signals (V_{C1}, V_{C2}, and V_{C3}) with a memory cell to switch the logic functions, one output signal (V_{OUT}), and a switch signal (V_{SW}) to perform Floating Gate Calibration (FGC) operation. And the configuration is a combination of 7-input νCMOS$_{P1}$, 6-input νCMOS$_{P2}$, and 8-input νCMOS$_{M}$. Each νCMOS has an FGC circuit to cancel the effect of a charge accumulated in the FG. FG$_{P1}$, FG$_{P2}$, and FG$_{M}$ are FGs of each CMOS. C_{P11} to C_{P17} are the gate capacitances of νCMOS$_{P1}$, C_{P21} to C_{P26} are the gate

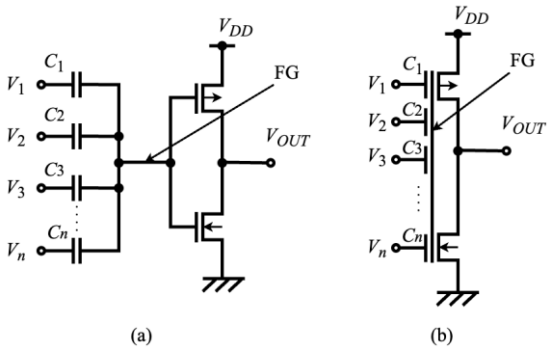


Fig. 2. (a)Circuit diagram and (b)Circuit symbol of neuron CMOS inverter

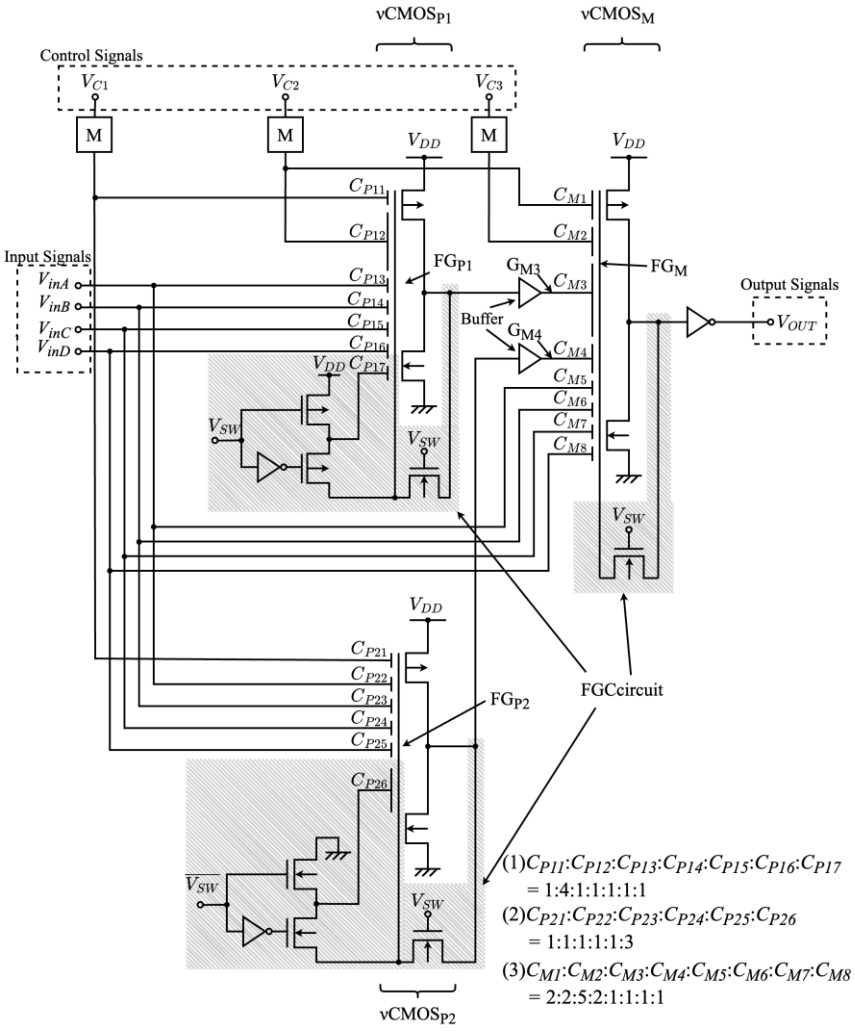


Fig. 3. Circuit diagram of 4-input Variable Logic circuit using neuron CMOS inverters

capacitances of νCMOS$_{P2}$, and C_{M1} to C_{M8} are the gate capacitances of νCMOS$_M$. The capacitances ratio of νCMOS$_{P1}$ is C_{P11}:C_{P12}:C_{P13}:C_{P14}:C_{P15}:C_{P16}:C_{P17} = 1:4:1:1:1:1:1. The capacitances ratio of νCMOS$_{P2}$ is C_{P21}:C_{P22}:C_{P23}:C_{P24}:C_{P25}:C_{P26} = 1:1:1:1:1:3. The capacitances ratio of νCMOS$_M$ is C_{M1}:C_{M2}:C_{M3}:C_{M4}:C_{M5}:C_{M6}:C_{M7}:C_{M8} = 2:2:5:2:1:1:1:1[7]. The inversion threshold voltage of each νCMOS is V_{DD} / 2.

The 4-νVLC realizes eight symmetric logic functions, as shown in TABLE I. In TABLE I, (b)Tautology means V_{OUT} is always "1", and (g)Inconsistency means V_{OUT} is always "0". The operation of the circuit has two stages: an FGC operation and variable logic operations, and variable logic operations follow the FGC operation. In the FGC operation, V_{SW} is set to "1", the three control signals are set to "1", and the four input signals are set to "0" to eliminate the effect of the charge accumulated in FG. It is noted that "0" is 0 [V] in binary, and "1" is V_{DD} [V]. In the variable logic operations, after V_{SW} is set to "0", the control signals V_{C1}, V_{C2}, and V_{C3} are assigned to the values corresponding to the logic functions listed in TABLE I. The output signal for the input signals is obtained from the selected logic function.

Fig. 4 shows the theoretical performance of ν CMOSM when selecting the XNOR function with the Floating-Gate Potential Diagram (FPD) [8] [9]. FPD is used very extensively in the design and analysis of νCMOS circuits. In Fig. 4, the horizontal line V_i is given by (V_{inA} + V_{inB} + V_{inC} + V_{inD}) / 15 and is expressed based on the number of "1"s. The vertical line $V(FG_M)$ is the potential of FG$_M$. When all the input gate voltages of νCMOS$_M$ are "1", $V(FG_M)$ is the highest value (upper limit of the vertical line), and when all the input gate voltages of CMOS$_M$ are "0", $V(FG_M)$ is the lowest value (lower limit of the vertical line). C_T is the total combined capacitance of νCMOS$_M$, C_T = C_{M1} + C_{M2} + ... + C_{M8}. The circuit is set to C_{M5} = C_{M6} = C_{M7} = C_{M8} to handle symmetric functions. The baseline in Fig. 4 shows the characteristic of $V(FG_M)$ concerning V_i when V_{C2}, V_{C3}, $V(G_{M3})$, and $V(G_{M4})$ are all "0". When the $V(FG_M)$ value (thick line) is larger than V_{DD} / 2 (dashed line), the output voltage V_{OUT} is "1". When the $V(FG_M)$ value (thick line) is lower than V_{DD} / 2 (dashed line), V_{OUT} is "0".

First, it is exemplified that the function of XNOR is obtained from the capacitance ratios of (1), (2), and (3) in Fig. 2, with FPD. Assuming that the unit capacity is C, C_{M5} = C_{M6} = C_{M7} = C_{M8} = C/15, and the maximum value of the baseline in Fig. 4 is 4C/15. Next, Fig. 4 shows that when V_{C2} and V_{C3} are "1", $V(FG_M)$ increases from baseline by 4C/15, the capacitance values of C_{M1} and C_{M2}. V_{INVP1} and V_{INVP2} are the apparent inversion threshold voltages seen from V_i of νCMOS$_{P1}$ and νCMOS$_{P2}$, which are designed to be 0.5V_{DD} / 15 and 2.5V_{DD} / 15. Then, a thick line in Fig. 4 can be drawn based on these two thresholds and the slope of the baseline. Therefore, the XNOR function can be realized by changing the values of control signals, and seven types of logical functions other than XNOR can be realized similarly.

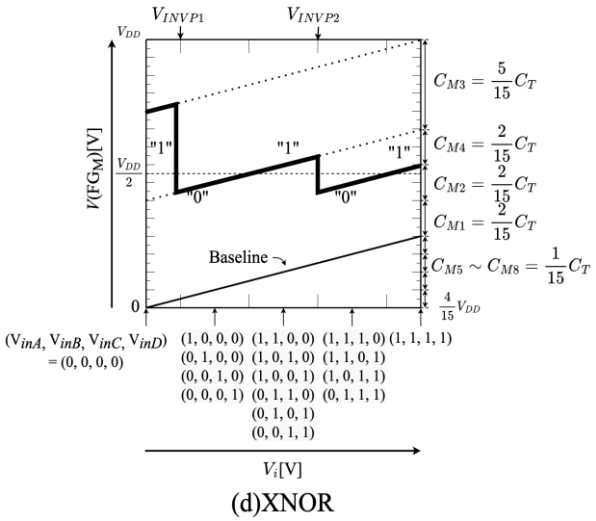
Next, HSPICE simulations confirm that the 4-νVLC realizes the eight symmetric logic functions. Fig. 5 shows the results of the HSPICE simulations using the Rohm 0.18μm process and the device parameters in TABLE II. The waveforms are V_{SW}, V_{C1}, V_{C2}, V_{C3}, V_{inA}, V_{inB}, V_{inC}, V_{inD}, and V_{OUT} from top to bottom, and the vertical line is "voltage, V" and the horizontal line is "second, s". It can be observed that the eight logic functions shown in TABLE I are obtained by

TABLE I. SIGNAL TABLE

FGC Operation (V_{SW} = "1")						
Control signals			Input signals			
V_{C1}	V_{C2}	V_{C3}	*VinA*	*VinB*	*VinC*	*VinD*
1	1	1	0	0	0	0

Variable logic Operation (V_{SW} = "0")			
Control signals			Logic Function
V_{C1}	V_{C2}	V_{C3}	
0	0	0	(a)OR
0	0	1	(b)Tautology*
0	1	0	(c)NOR
0	1	1	(d)XNOR
1	0	0	(e)XOR
1	0	1	(f)NAND
1	1	0	(g)Inconsistency*
1	1	1	(h)AND

*(b)Tautology means V_{OUT} is always "1",
(g)Inconsistency means V_{OUT} is always "0"



(d)XNOR

Fig. 4. Floating-Gate Potential Diagram of νCMOS$_M$ in 4-νVLC

TABLE II. DEVICE PARAMETERS AND SIMULATION CONDITIONS

Symbol	Value	Units
V_{DD}	1.8	V
GND	0	V
C	16	fF
W_n/L_n	0.8/0.2	μm
W_p/L_p	3.0/0.2	μm

changing the values of the three control signals. In period (d) of Fig. 5, the output signal is "1" when the number of "1"s of the input signals is even, such as (V_{inA}, V_{inB}, V_{inC}, V_{inD}) = (0, 0, 0, 0), V_{OUT} = "1", (V_{inA}, V_{inB}, V_{inC}, V_{inD}) = (1, 0, 0, 0), V_{OUT} = "0". This is the same behavior as in Fig. 4 and shows that the XNOR function is realized.

C. Basic Logic Element

FPGAs have BLEs, as shown in Fig. 6(a)[1], and the BLE consists of a LUT, a D-FF, and a selector. The selector has a memory cell, M in Fig. 6, to determine whether to output the LUT value as is or store it once in the D-FF. The 4-LUT, as shown in Fig. 6(b), realizes sixteen logic functions by storing the output values corresponding to the desired logic functions in sixteen memory cells, M0 to M15. The 4-LUT provides the AND function for four input signals by setting memory cells such as (M0, M1, M2, M3, M4, M5, M6, M7, M8, M9, M10, M11, M12, M13, M14, M15) = (1, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0). For example, when (VinA, VinB, VinC, VinD) =

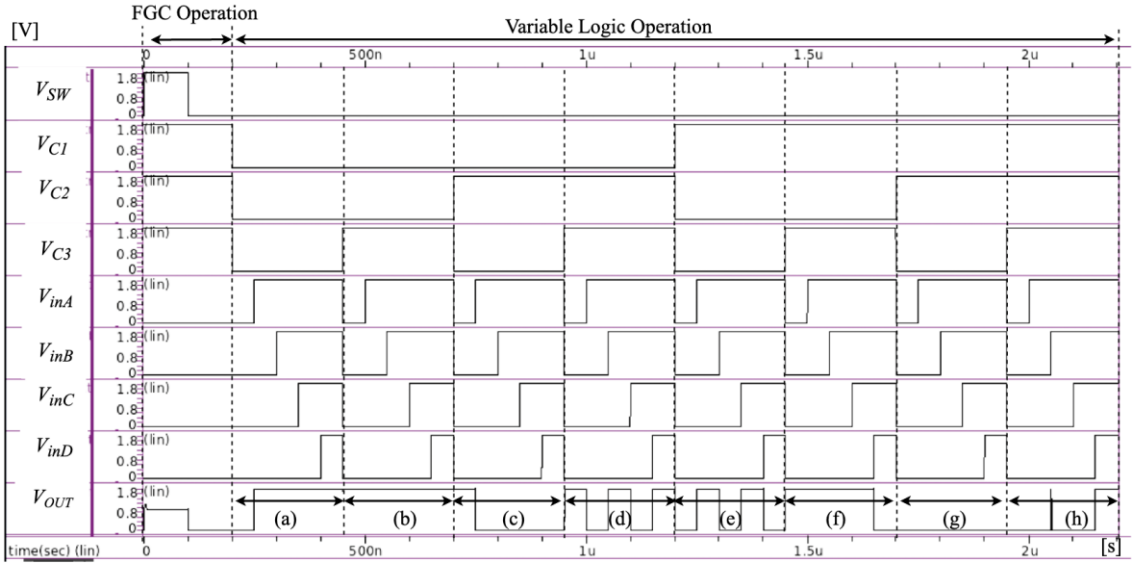


Fig. 5. Simulation waveforms for eight logic functions of 4-vVLC

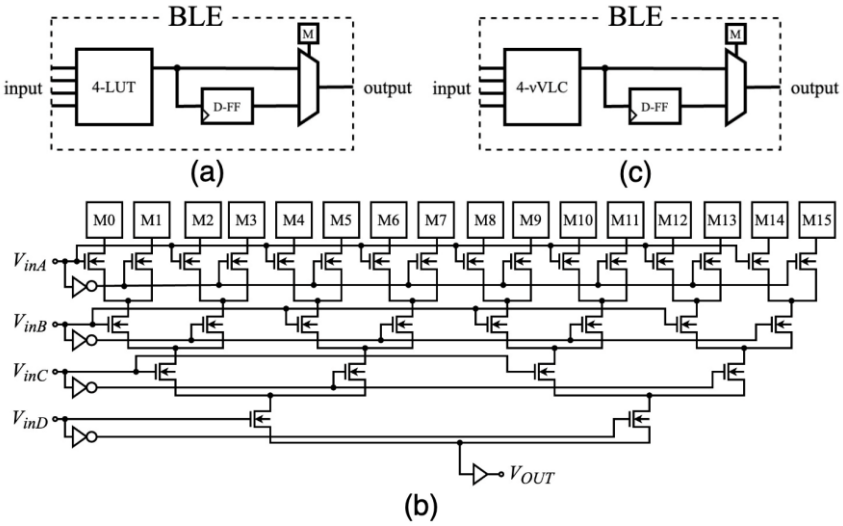


Fig. 6. Circuit diagram of (a)ordinary BLE, (b) 4-LUT, and (c)BLE using 4-vVLC

(1, 1, 1, 1), V_{OUT} is "1" which is the value of M0. In comparison, the 4-vVLC realizes eight symmetrical logic functions by switching three control signals with a memory cell. Fig. 6(c) shows the BLE using the 4-vVLC instead of the 4-LUT.

III. Evaluation

In this evaluation, the 4-LUT and the 4-vVLC are compared based on circuit operations by HSPICE simulations and layout areas. The parameters in TABLE II and the Rohm0.18 process were used for the HSPICE simulations and layout designs.

A. HSPICE simulations

Fig. 7 shows the HSPICE simulation waveforms that is the XNOR behavior of the 4-LUT and the 4-vVLC. The waveforms are V_{SW}, V_{C1}, V_{C2}, V_{C3}, V_{inA}, V_{inB}, V_{inC}, V_{inD}, Output of 4-vVLC, and Output of 4-LUT from top to bottom, and the vertical line is "voltage, V" and the horizontal line is "second, s". The 4-LUT provides the XNOR function for four input signals by setting memory cells such as (M0, M1, M2, M3, M4, M5, M6, M7, M8, M9, M10, M11, M12, M13, M14, M15) = (1, 0, 0, 1, 0, 1, 1, 0, 0, 1, 1, 0, 1, 0, 0, 1). The 4-vVLC operates the behavior of XNOR corresponding to the four input signals by setting $V_{sw} = 0$, (V_{C1}, V_{C2}, V_{C3}) = (0, 1, 1) after the FGC operation, thereby obtaining in general agreement as the operation of the 4-LUT

B. Layout area

We designed the circuit layouts of the 4-LUT, 4-vVLC, the BLE using 4-LUT, and the BLE using 4-vVLC in Fig. 8, and we have calculated the length times width multiplication from Fig. 8 to measure the layout areas and filled the values of layout areas obtained from the above calculations into TABLE III. The TABLE III shows the number of transistors and memory cells in addition to layout areas of the 4-LUT, the 4-vVLC, the BLE using 4-LUT, and the BLE using 4-vVLC, respectively. According to TABLE III, as the layout of 4-LUT is 4841.60 μm^2 and the layout area of 4-vVLC is 4670.64 μm^2, we know that the layout area of the proposed 4-vVLC is reduced by about 3.5% from the conventional 4-LUT. In addition, the layout area of BLE using 4-LUT is 6197.12μm^2, and the layout area of BLE using the 4-vVLC is 5968.04μm^2, meaning that the layout area is reduced by about 3.7%. The layout area of 4-vVLC is smaller than that of 4-LUT because

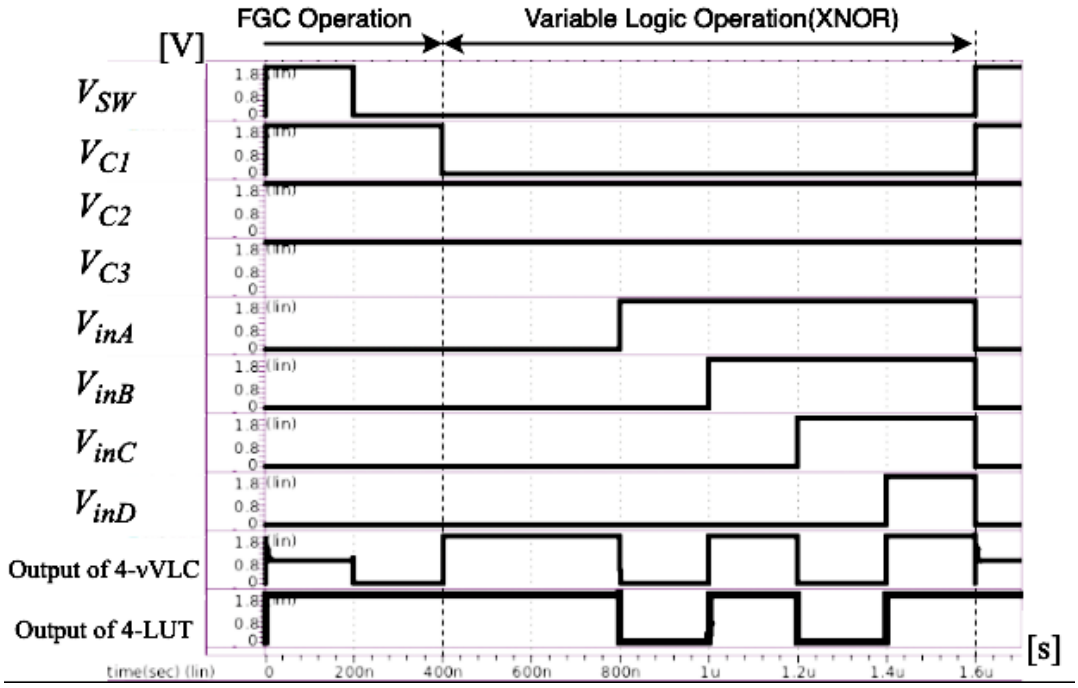


Fig. 7. Simulation waveforms of 4-LUT and 4-vVLC XNOR operation

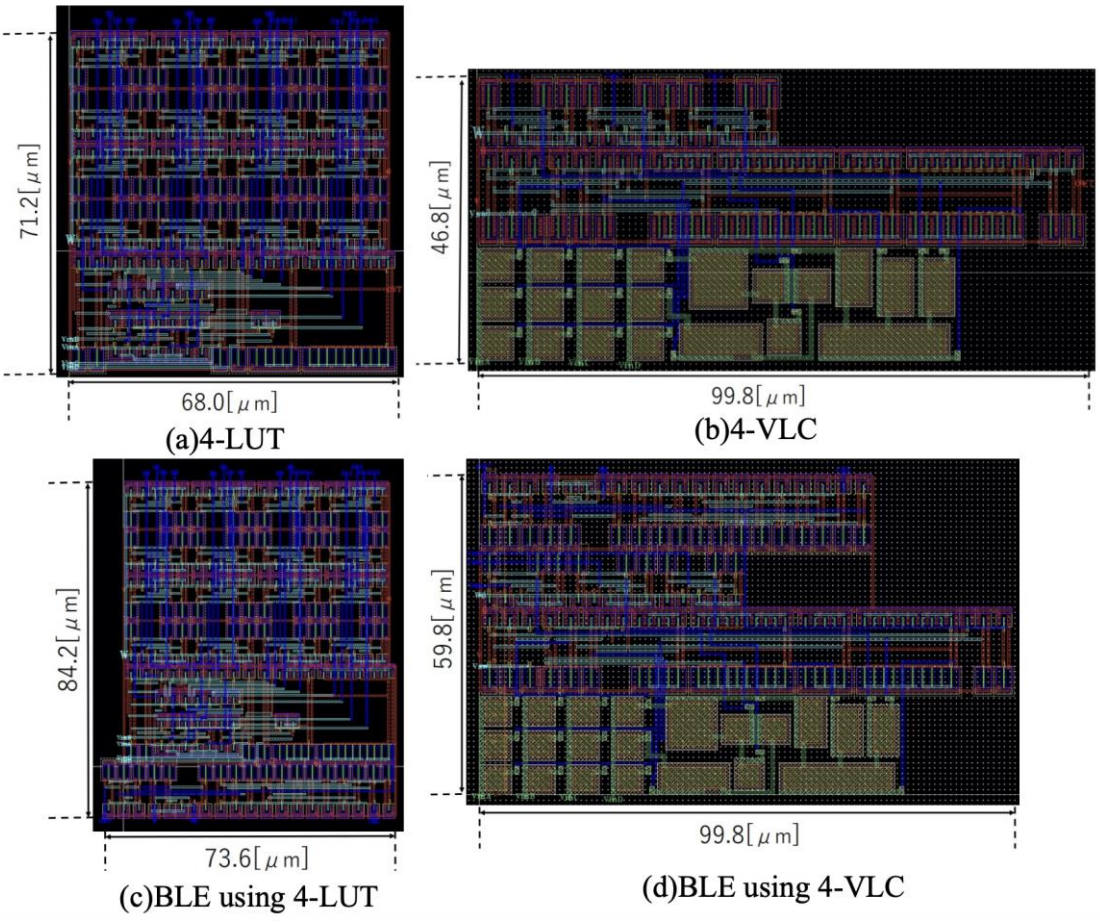


Fig. 8. Layout design of (a) 4-LUT, (b) 4-vVLC, (c) BLE using 4-LUT, and (d) BLE using 4-vVLC

TABLE III. SUMMARY OF LAYOUT AREA, THE NUMBER OF TRANSISTORS , AND THE NUMBER OF MEMORY CELLS

$$*Reduction\ ratio = \left(1 - \frac{layout\ area\ of\ 4{-}\nu VLC}{layout\ area\ of\ 4{-}LUT}\right) \times 100\ [\%]$$

$$**Reduction\ ratio = \left(1 - \frac{layout\ area\ of\ BLE\ using\ 4{-}\nu VLC}{layout\ area\ of\ BLE\ using\ 4{-}LUT}\right) \times 100\ [\%]$$

	The number of memory cells	The number of transistors	Layout Area [μm^2]	Reduction ratio [%]
4-LUT	16	170	4841.60	3.5 (*)
4-νVLC	3	47	4670.64	
BLE using 4-LUT	17	208	6197.12	3.7 (**)
BLE using 4-νVLC	4	85	5968.04	

there are fewer memory cells, although the 4-νVLC uses 21 capacitors.

To measure the layout areas, we have calculated the length of the layouts by the width of the layouts multiplication. As the layout area in Fig. 8 includes the layout spots with no circuits, it is possible to reduce the area more by devising the layout design like a rectangle shape.

C. The number of memory cells and transistors

The number of memory cells in the 4-LUT and the 4-νVLC in TABLE III can be filled in from the circuit diagram of the 4-νVLC, Fig. 3, and the circuit diagram of the 4-LUT, Fig. 6, as follows: the number of memory cells in the 4-νVLC is three and the number of memory cells in the 4-LUT is sixteen. In addition, from Fig. 6(a) and 6(b), the number of memory cells in the BLE using the 4-LUT and the BLE using the 4-νVLC can be filled in as four and seventeen, respectively, since the number of memory cells in the selector is added to the number of memory cells in the 4-LUT and 4-νVLC, respectively. Additionally, the number of transistors in 4-LUT, 4-VLC, BLE using 4-LUT, and BLE using 4-VLC are 170, 47, 208, and 85, respectively.

IV. DISCUSSION

As discussed in Section III, the usage of νVLC could reduce the layout area of the BLEs, but the reduction ratio is not very high. We consider that the interconnect capacitance could be used to the νVLC to reduce the layout area of the BLEs further. A layout design using Metal-Insulator-Metal (MIM) capacitors tends to increase the area due to design rules. We have studied the νCMOS, which uses interconnect capacitance instead of MIM capacitors [10]. Therefore, it is possible to reduce the area of the 4-νVLC more by using interconnect capacitance.

V. CONCLUSION

In this paper, we describe the circuit configuration and operations of 4-νVLC, and have verified that the waveforms of the HSPICE simulations and the theoretical results with the FPD are in general agreement. In addition, we have designed the layout of the BLEs with the 4-LUT and 4-νVLC, respectively, and evaluated those layout areas. We show that the layout area of BLE with 4-νVLC is less than the layout area of BLE with 4-LUT because the number of memory cells of BLE with 4-νVLC is three against the number of memory cells of BLE with 4-LUT is sixteen. The layout area of the 4-νVLC is reduced by about 3.5% compared to the 4-LUT, and the layout area of BLE using the 4-νVLC is reduced by about 3.7% compared to BLE using the 4-LUT.

In future works, we will consider using interconnect capacitance instead of MIM capacitors in νCMOS to reduce the BLE area. In addition, we will make each νCMOS on a chip to realize 4-νVLC operations in actual devices and will evaluate the behavior regards on the chip.

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