A Design of Low Voltage Spacer Detector Circuits for Asynchronous Ternary Logic System

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***Abstract*—The ternary logic approach was proposed in an asynchronous digital system to eliminate overhead wires for communication signals in preference to the binary logic approach. Spacer detectors (SDs) are crucial in ternary logic to determine whether or not the input voltage is equivalent to empty. The Internet of Things (IoT) devices leverage asynchronous multi-value logic systems for machine learning inference to minimize power consumption. These IoT devices are also expected to operate at ultra-low operating voltages (sub- or near-threshold voltages). An ultra-low supply voltage restricts the operation of the SD circuit because of the need to determine the space value with a logical intermediate value. This study presented SD circuits was applied a pseudo-differential amplifier instead of the traditional element-based inverter circuit to design H-element and L-element. Hence, our proposed SD circuits can operate at low supply voltage without body bias using a bulk-controlled method. The proposed circuit was simulated in 65 nm UMC LL process technology in the Cadence Virtuoso analogue design environment with power consumption compared with the difference in supply voltage from 0.35 to 0.9 volts.**

***Index Terms*—asynchronous circuits, ternary logic, spacer detector**

I. Introduction

An asynchronous digital system called self-time circuitry operates independently of the global clock system to reduce skew and minimize dynamic power dissipation. Asynchronous systems require the handshaking protocol for communication among various modules of the circuit in the form of requests and acknowledgements signal and additional wire for caring data [1]. For example, the four-phase dual-rail protocol design is a commonly used approach. It involves a 2-phase handshake signal and utilizes a 2-rail protocol to encode both request signals and acknowledgements with each data bit. In addition, the protocol is coupled with the dual-rail data encoding technique, which requires the deployment of a pair of wires for transmitting one-bit data. As a consequence, there would be a significant increase in the number of communication wires and the intricacy of routing on-chip networks of communication [2], [3].

Multi-valued logic (MVL) approaches have been proposed to alleviate this drawback, with particular emphasis on circuits utilizing ternary logic [4]. Fig.1 shows the ternary encoding convention employing a tripartite logic system. High voltage represents the binary logic state "1" and low voltage represents the binary logic state "0", with a logical intermediate value ($vdd/2$) representing the invalid data called spacer as communication between the combination circuitry. Spacer detectors (SDs) are essential components for determining whether or not the input voltage is equal to the spacer. Consequently, all inputs were connected to the SDs, with outputs of the SDs connected to the NOR gate, as shown in Fig. 2, and the output of the combination circuit controlled by the B and S signals [5], [6].

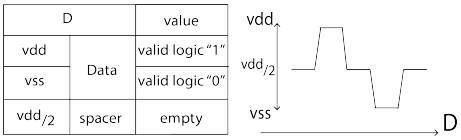

Fig. 1. The ternary data encoding for asynchronous system.

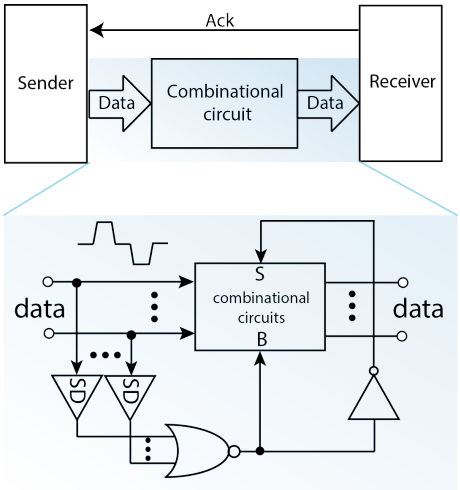

Fig. 2. Principle of asynchronous ternary combinational circuit with spacer detectors

The spacer detectors (SDs) were designed based on an inverter circuit comprising pMOS and nMOS transistors. This particular circuit presented a logical intermediate value that was difficult to handle as it exceeded the threshold voltages of pMOS and nMOS transistors. Consequently, both pMOS and nMOS transitors were triggered into an ON state. Adjusted transistors sizing is a technique for designing SD-based inverter circuits. In [7], the SD circuit was presented with two different power supplies (e.g., $vdd/2$ and vdd) that reduce the current draw from the power supply. The SDs

circuit with reverse body bias (RBB) [8] proposed to decrease static power consumption.

In the AI-enabled IoT devices era, asynchronous digital system is an attractive schemes for IoT application that can perform machine learning (ML) algorithm.,while AIoT devices expected to have a long service lives. [9] presented an asynchronous circuit design using the full diffusion and UMC LL 65 nm technology that can perform the TM (Tsetlin Machine) algorithm with a 0.25 to 1.2 supply voltage.

Internet of Things (IoT) devices can decrease their operating voltage to migrate power consumption through CMOS technology downscaling, while the threshold voltage is not substantially reduced [10]. In [11] presented a binary logic to multi-valued logic (MVL) circuit converter in 32 nm TSMC CMOS technology, where the operating voltage did not fall below 0.3 volts. Their proposed circuit reduced the power consumption compared with the 180 nm TSMC CMOS implementation. However, the spacer detector is a necessary part which controls the MVL signal and no mechanism has been presented for this to operate at a sub- or near-threshold voltage while utilizing a sole supply voltage.

This study introduced a new spacer detector, designed for asynchronous ternary logic, to achieve sub- or near-threshold voltage operation without body-bias technique. The circuit design was simulated using the 65 nm UMC LL process technology, operated with a supply voltage ranging from 0.35 to 0.9 volts in the Cadence Virtuoso analog design environment. The remainder of this paper is organized as follows: Section II describes the proposed spacer detector, comprising H-element and L-element circuits. Section III discusses the experimental results, with conclusions drawn in Section IV.

II. A PROPOSED SPACER DETECTOR

Fig.3 shows the components of the SD circuit, with the H-element and the L-element connected to the binary XOR and the output determining whether or not the input signal is a spacer signal. If the input signal is a spacer, then S will be logic "1" with SN indicating the data of the input signal. Binary XOR was implemented using transmission gate Logic. In this section introduces the new H-element and L-element circuits that operate in the same way as the conventional inverter one [7].

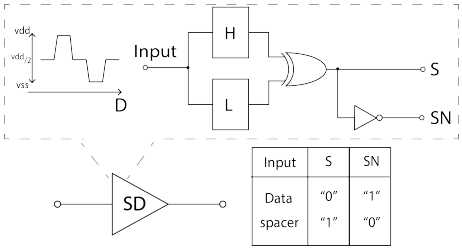

Fig. 3. Space detector circuit with its functional output.

A. H-element

The main part of the H-element is based on a pseudo-differential amplifier that lacks a tail current source; thus, it can operate at a low supply voltage [12], as shown in Fig. 4. The H-element generates a logical output of "1" when the input signal value exceeds $vdd/2$ or logical middle value. In this case, the current mirror is constituted by the nMOS transistors, whereas the pMOS transistor M_6 serves as the input transistor, which turn ON state when the input signal voltage exceeds zero. This pMOS transistor also operates as a differential amplifier.

The output of the pseudo-differential amplifier is connected via a negative feedback loop to the pseudo-PMOS inverter, which provides voltage bias to the pMOS transistor M_1 together with nMOS transistor M_2 connected to supply voltage instead of resistor, thereby reducing area cost.

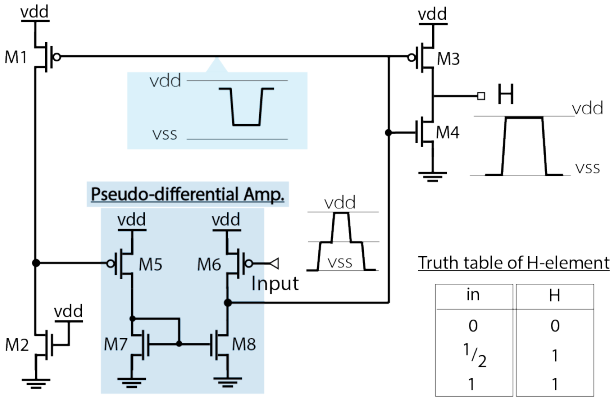

Fig. 4. Schematic of proposed H-element circuits and its operation.

When the low input voltage is fed to pMOS transistor M_6, pMOS transistor M_1 turns on, and the output of the pseudo-PMOS inverter generates a high input voltage for pMOS transistor M_5. Consequently, the pseudo-differential amplifier generates a high output voltage. Conversely,when the pseudo-differential amplifier generates a low output voltage. The pMOS transistor M_6 receives an input voltage that exceeds $vdd/2$, while the pMOS transistor M_5 experiences a lower input voltage compared to M_6. The output signal is then inverted by the inverter, while the output voltage swings from rail-to-rail.

B. L-element

The main part of the L-element is also based on a pseudo-differential amplifier, as shown in Fig. 5. L-element generate a logical output of "1" when the input signal value is high compared to supply voltage. In this case, the current mirror is constituted by the pMOS transistors, whereas the nMOS transistor M_{14} serves as the input transistor, which turn ON state when the input signal nears supply voltage. This nMOS transistor operates as a differential amplifier.

The L-element has a similar function to the H-element when both inputs of the pseudo-differential amplifier are not equivalent and the output swings up or down depending on the input voltage value of the nMOS transistor M_{13}. The pseudo-differential amplifier generates a low output voltage when the nMOS transistor M_{14} receives a nominal input voltage. The output signal is inverted by the inverter, while the output voltage swings from rail-to-rail.

III. RESULTS AND ANALYSIS

The proposed SD circuit was designed and simulated to confirm operation, power consumption and frequency

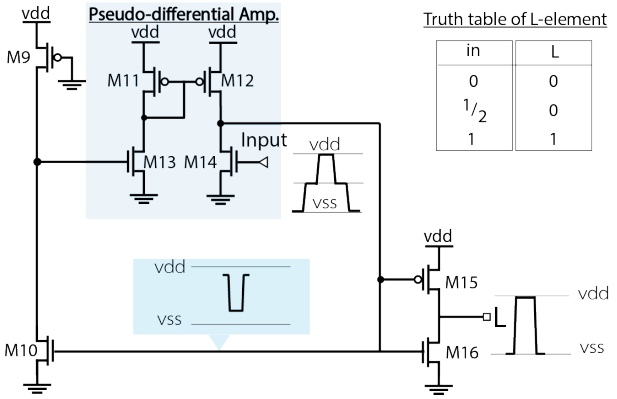

Fig. 5. Schematic of proposed L-element circuit and its operation.

stability as jitter by Cadence Spectre, with simulation results based on a typical process corner and a temperature of 27 °C. All the lengths of transistors were 65 nm, with the widths of the transistors in the H- and L-elements shown in Table 1. The threshold voltage of the pMOS transistor was 0.45 volts, while that of the nMOS was 0.54 volts. Therefore, 0.5 volts was near-threshold voltage.

TABLE I
SIZE OF TRANSISTOR USED IN SD CIRCUIT

H-element		L-element	
transistor	w(um)	transistor	w(um)
M1	2.20	M9	0.64
M2	0.64	M10	2.2
M3,M4	4	M11,M12	2.7
M5,M6	2.7	M13,M14	1.8
M7,M8	1.8	M15,M16	4

A. *Functional simulation results*

The voltage transfer curve (VTC) simulation results of the SD circuit with a 0.35 – 0.5 supply voltage and a 0.5 – 0.9 supply voltage are shown in Fig. 6, and Fig. 7 respectively. The output of the H-element and L-element results in a waveform, which is correct operation.

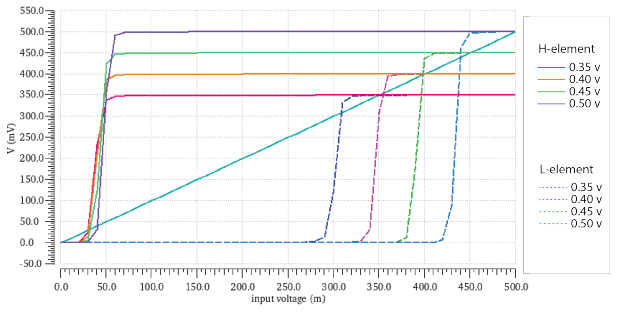

Fig. 6. The voltage transfer curve (VTC) simulation results of the SD circuit with sub- or near-threshold supply voltage.

The circuit operation corresponding output waveform was also simulated to confirm the transient analysis. The input waveform followed ternary logic (0 → 1/2 → 1 → 1/2 → 0), with logical intermediate value and supply voltage value corresponding as logic "1" to give the input signal,

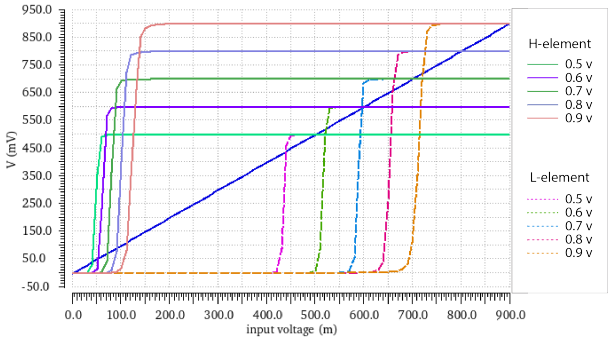

Fig. 7. The voltage transfer curve (VTC) simulation results of the SD circuit with near-threshold and nominal supply voltage.

with a period of more than 0.1 μs. The SD circuit with a sub- or near-threshold supply voltage responded well with a low-frequency value, i.e., a long time period. The output waveforms of the L-element and H-element circuits are shown in Fig. 8, with the output waveforms of S and SN shown in Fig. 9.

On the other hand, the SD circuit with a near-threshold and nominal supply voltage responded well with a high-frequency value, i.e., a short time period. The output waveforms of the L-element and H-element circuits are shown in Fig. 10, with output waveforms of S and SN shown in Fig. 11. The SD circuit at 0.5 operating voltage performed at either high- or low-frequency input signals.

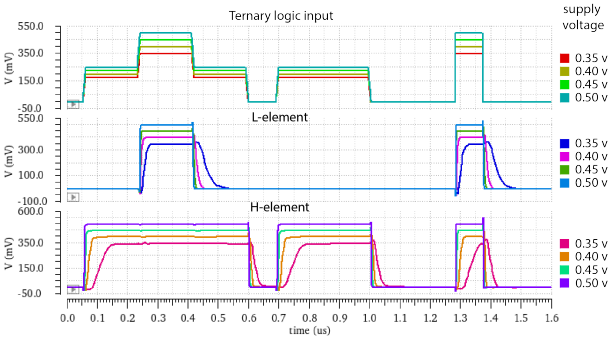

Fig. 8. The input waveform corresponding to low frequency and output waveform of the H- and L-element circuits exhibits an operation with a supply voltage ranging from 0.35 to 0.5 volts.

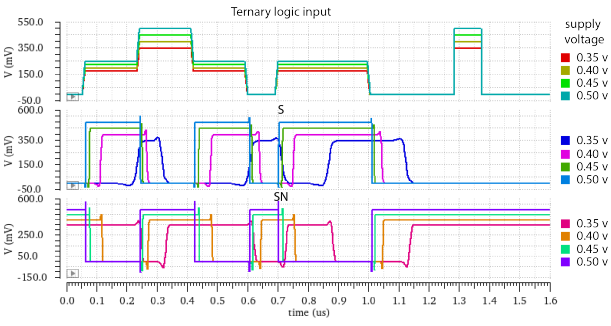

Fig. 9. The input waveform corresponding to low frequency and output waveform of the spacer detector exhibits an operation with a supply voltage ranging from 0.35 to 0.5 volts.

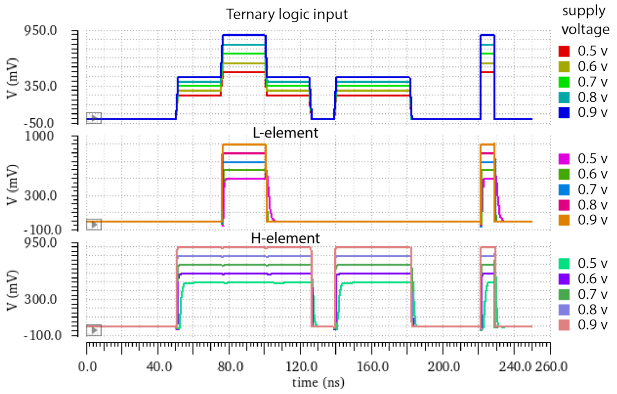

Fig. 10. The input waveform and output waveform of the H- and L-element circuits exhibit an operation with a supply voltage ranging from 0.5 to 0.9 volts.

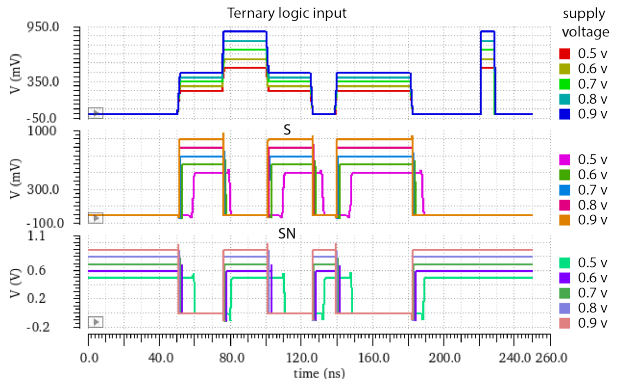

Fig. 11. The input waveform and output waveform of the spacer detector exhibits an operation with a supply voltage ranging from 0.5 to 0.9 volts.

B. Power and jitter simulation results

The power consumption of the SD circuit varied with the applied supply voltage, which ranged from 0.35 to 0.9 volts, as shown in Table II. The result was compared with the jitter value obtained result from a periodic steady-state analysis (PSS) in Cadence simulation. The jitter relates to the amount of stability exhibited by the output waveform in the temporal domain. Findings indicated a correlation between the supply voltage and jitter value in terms of trade-off performance.

IV. Conclusion

This paper presented a novel spacer detector that operated at sub- or near-threshold voltages and nominal voltages. The circuit was constructed by a pseudo-differential amplifier with a negative feedback loop that relied on pseudo-NMOS and PMOS inverters instead of resistive loads. Power consumption and area costs were substantially reduced when using this scheme.

TABLE II
THE POWER CONSUMPTION AND JITTER OF SD CIRCUIT WITH DIFFERENT SUPPLY VOLTAGE

Supply Voltage	Power (uW)	Jitter (ns)
0.35	0.082	54.41
0.40	0.309	0.115
0.45	1.093	0.062
0.50	3.329	0.037
0.60	18.27	0.0181
0.70	60.40	0.0117
0.80	144.6	0.0073
0.90	281.1	0.0059

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