An Exploration of the Effective Path for Current Conduction in a Triple Gate Junctionless FinFET

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***Abstract*—The goal of this work is to exclusively investigate the effective path for current conduction in the channel of a Triple Gate (TG) Silicon-ON-Insulator (SOI) Junctionless Fin Field Effect Transistor (JLFinFET). It is observed that various structural parameters play a key role in deciding the location of the effective current path both in full depletion mode and partial depletion mode in TG SOI JLFinFET. Considering the present day technology requirements 20 nm was chosen as the gate length. Simulations performed using 3-D TCAD namely ATLAS by Silvaco Inc. reveal that the conducting path from source to drain starts from nearer to the centre of the channel (i.e, at half the fin height and half the fin width) when the transistor switches from the OFF state to the ON state. It is also observed that when the triple gate transistor scales down in size the capacitive coupling between the top gate and side gates is a crucial factor in determining the location of the effective current path.**

***Index Terms*—Triple Gate, JLFinFET, Effective path for current conduction, Potential profile**

I. Introduction

To overcome the fundamental performance limits of the conventional Metal Oxide Semiconductor Field Effect Transistors (MOSFETs), different types of devices like FinFET, Tunnel FETs (TFET) and Impact Ionization Metal Oxide Semiconductor (IMOS) were developed [1]. These alternative options to the conventional MOSFET fundamentally need the composition of p-n junctions at the source-channel and channel–drain interface. However, scaling the devices to the deca-nanometer pose fabrication difficulties due to the requirement of steep doping gradients within a few nanometer wide channel region. A significant invention that has nullified the above mentioned fabrication difficulty was the Junctionless Field Effect Transistor (JLFET). JLFETs have a uniform doping concentration in the source-channel-drain region. The first JLFET with a silicon thickness of 10 nm and a channel length of 1 μm was fabricated in 2010 by J. P. Colinge et al., [2].

Unlike conventional Inversion Mode (IM) MOSFETs, the operation is different in JLFETs. Metal constituting gates have Fermi level lower than the Fermi level of silicon channel (for n-type transistor) which will deplete the channel region [1]. The triple gate architecture not only provides enhanced electrostatic control and reduced short-channel effects but also assists in the full depletion of the silicon channel as most of the silicon channel is surrounded by a metal gate. Hence in this work emphasis is made on studying the electrostatics in the channel region of Triple Gate Silicon-ON-Insulator Junctionless Fin Field Effect Transistor (TG SOI JLFinFET).

To understand the operation of the device, it is important to know about the conduction region formation in the device. Effective Path for Current Conduction (EPCC) is the path in the channel from source to drain where maximum current flows [3]. For conventional MOSFETs, the EPCC will be near the gate oxide-channel interface. Numerous research works had been published that give insight into the characteristics of TG SOI JLFinFET [3]–[5]. In all these published literature the EPCC was assumed to be near the BOX-channel interface. However in [6], J.P. Colinge et al., have demonstrated that for bulk Junctionless Nanowire Transistor (JNT) with lower dimensions current density will be maximum at the middle of the channel (half the fin height). Considering the current technology requirements, a deeper exploration of the location of the EPCC is essential for a better understanding of the device physics and thereby predicting the terminal characteristics accurately. Hence in this work, using suitable quantum models, analysis was done to examine the dependence of the location of the EPCC on various structural parameters like gate oxide material, gate oxide thickness, gate work function, width of the fin, length of the gate and height of the fin. Section II will give insight into the device structure and simulation set-up used. In section III, results for the simulated device are analysed and section IV will conclude the work.

II. Device structure and simulation specifications

The 3-D structure of the simulated n type TG SOI JLFinFET is shown in figure 1a. Figures 1b and 1c show the 2-D cross-sectional view of the device along the YZ plane and XZ plane respectively. The length of the gate is taken along the X-axis, the width of the fin is taken along the Y-axis, and the height of the fin is taken along Z-axis. The origin is denoted by O (0, 0, 0) and is indicated in figure 1a. Unless stated otherwise, the parameter values used for the device simulation are listed in Table I. The source of the channel is located at $L_g = 0$ nm, the drain is located at $L_g = 20$ nm. SiO_2 is chosen for gate oxide as well as buried oxide. The device is simulated with the given parameters in 3-D TCAD device simulator namely ATLAS by Silvaco Inc. CVT and fldmob mobility models are used for transverse and lateral field dependent mobility effects respectively [7]. Unlike in conventional IM devices,

the electric field is relatively lower during on-state in JLFETs [8]. So a low-field mobility model, shiramob is included in the simulation. Leakage currents were taken into consideration in the simulation by including SRH recombination/generation model. A semiclassical model, dd_ms is used to capture quantum effects in the transverse direction while solving the schrodinger equations.

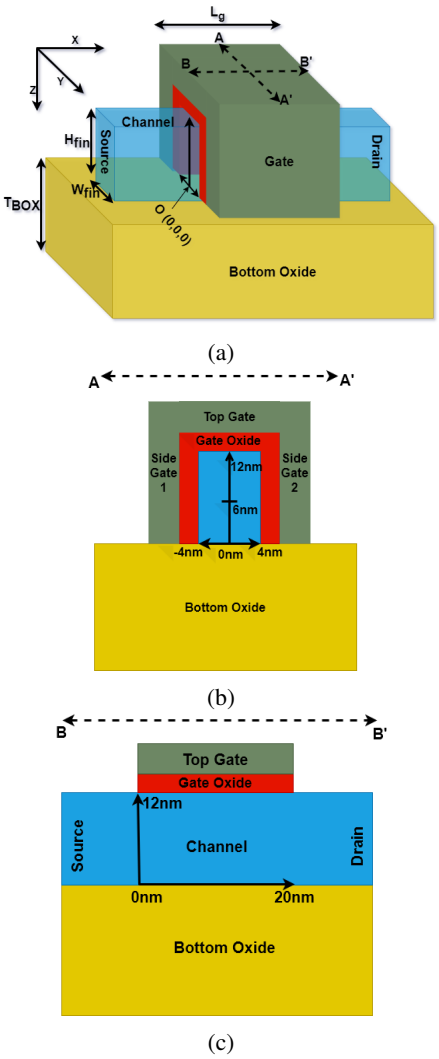


Fig. 1: (a) 3-D structure of the TG SOI JLFinFET, (b) 2-D cross sectional view of the device along cutline A-A', and (c) 2-D cross sectional view of the device along cutline B-B'

III. Results and Discussions

This section deals with two key aspects that shed light on the electrostatics in the conduction channel of TG SOI JLFinFET. The prime focus is given to analyzing the potential and electron concentration distributions and thereby locating the EPCC under various scenarios. It may be noted that the EPCC from source to drain is located at the maximum potential point both in the Y and Z directions. The impact of various transistor structural parameters on the location of EPCC is also dealt with in detail in this section.

TABLE I: Parameter specifications of TG SOI JLFinFET

Parameter	Value
Total gate length (L_g)	20 nm
Silicon film height (H_{fin})	12 nm
Silicon film width (W_{fin})	8 nm
Gate oxide thickness (t_{ox})	1.5 nm
Buried oxide thickness (T_{BOX})	12 nm
Doping concentration (N_d)	10^{19} cm^{-3}
Gate work function (ϕ_m)	5.25 eV

A. Electron Concentration and Potential Distribution at Different Locations in the Channel of TG SOI JLFinFET

1) Variation of Electron Concentration and Potential Along the Height of the Channel: Figure 2 depicts the variation of electron concentration with respect to gate voltage (V_g) at different heights of the channel (Z = 1 nm, 3 nm, 6 nm, 9 nm, and 11 nm) at the middle of the channel length (i.e. at X = 10 nm) and the middle of the fin width (i.e. at Y = 0 nm). To provide an idea of the different locations of Z, an inset of a 2-D cross-sectional view of the device along the YZ plane with markings at Z = 1 nm, 6 nm, and 11 nm is included at the top right corner of the figure. The drain voltage in all the simulations is fixed to 0.5 V. It can be observed that when the gate voltage is significantly low (i.e. in the full depletion mode of the transistor) the electron concentration is maximum at a height of 3 nm from the BOX-channel interface. When the transistor enters into partial depletion mode (i.e. $V_g > 0.75$ V) it is observed that the electron concentration is maximum in the region from Z = 3 nm to Z = 6 nm. However, when the transistor starts approaching the flatband mode (i.e. V_g = 1.2 V) electron concentration is equal throughout the channel indicating the presence of a completely neutral silicon channel without any depletion region. To analyze the distribution of potential in the channel of TG SOI JLFinFET from source to drain under various gate biases and heights, potential plots were taken along a cutline in the X direction at Y = 0 nm. This is illustrated in figure 3. It can be observed that for $V_g = 0$ V, the potential at Z = 1 nm and Z = 6 nm is higher than the potential at Z = 11 nm throughout the length of the channel indicating the influence of the gate material in strongly depleting the regions which are in proximity to the gate. For $V_g = 0.6$ V (i.e. when the transistor starts to enter into partial depletion mode from full depletion mode) the potential at Z = 6 nm is higher than the potential at Z = 1 nm and Z = 11 nm. This indicates that when the gate voltage approaches threshold voltage the maximum potential point (location of EPCC) shifts towards the middle of the channel. This can be attributed to the fact that for transistors with smaller device dimensions, the capacitive coupling due to the side gates as well as the top gate contributes to depleting the semiconductor region closer to the BOX-channel interface. Hence with the increase in gate bias conduction channel forms at the region close to the middle of

the channel (i.e. at $H_{fin}/2$). It is evident in the figure 4 which is a potential contour plot in the XZ plane at Y = 0 nm for V_g = 0.6 V that the potential is also maximum at the middle of the height of the channel. At $V_g = 1.2$ V (i.e. flatband condition), the entire channel along the height has the same potential. Hence the potential distribution at Z = 1 nm, 6 nm, and 11 nm are almost equal as seen from figure 3.

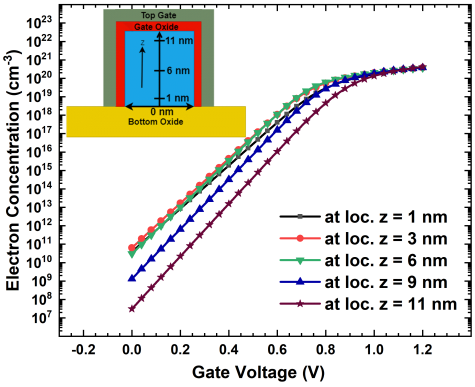


Fig. 2: Electron concentration versus gate voltage in the channel at various heights for $V_{ds} = 0.5$ V at $L_g/2$ (i.e. at X = 10 nm) and $W_{fin}/2$ (i.e. at Y = 0 nm).

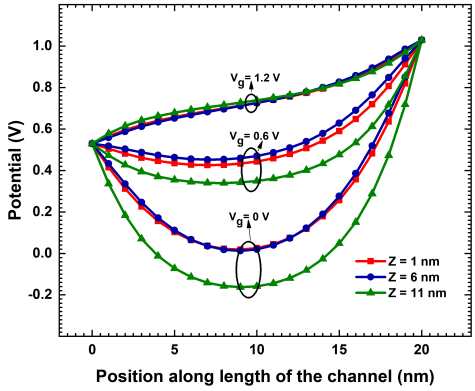


Fig. 3: Potential versus position along the length of the channel at various heights and various gate voltages for $V_{ds} = 0.5$ V at $W_{fin}/2$ (i.e. at Y = 0 nm).

2) Variation of Electron Concentration and Potential Along the Width of the Channel: Figure 5 depicts the variation of electron concentration with respect to gate voltage at different widths of the channel (Y = -4 nm, -2 nm, 0 nm, 2 nm, 4 nm) at the middle of the channel length (i.e. at X = 10 nm) and the middle of the fin height (i.e. at Z = 6 nm). To provide an idea of the different locations of Y, an inset of a 2-D cross-sectional view of the device along the YZ plane with markings at Y = -4 nm, 0 nm, and 4 nm is included at the top right corner of

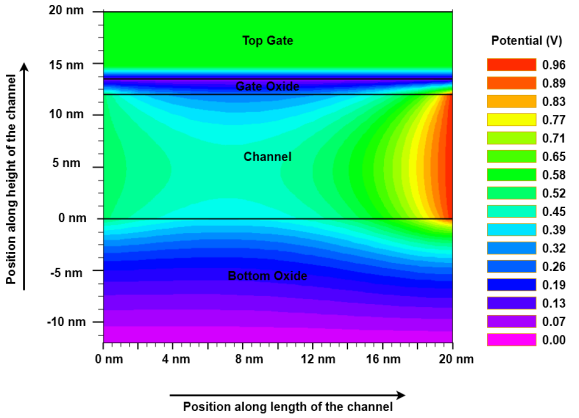


Fig. 4: Potential contour in XZ plane at $V_g = 0.6$ V for $V_{ds} = 0.5$ V, at $W_{fin}/2$ (i.e. at Y = 0 nm).

the figure. It can be observed that when the transistor is in full depletion and partial depletion modes (i.e. when $V_g < 1.1$ V) the electron concentration is maximum at the middle of the width of the channel as the gate influence is least at the middle of the width of the channel. It may be noted that the electron concentration at Y = -4 nm and -2 nm is exactly the same as that of at Y = 4 nm and 2 nm respectively because of the symmetrical gate structure along the width of the fin. However in figure 5, when the transistor reaches flatband mode (i.e. V_g = 1.2 V) electron concentration is equal throughout the channel indicating the presence of a completely neutral silicon channel without any depletion region. To inspect the distribution of

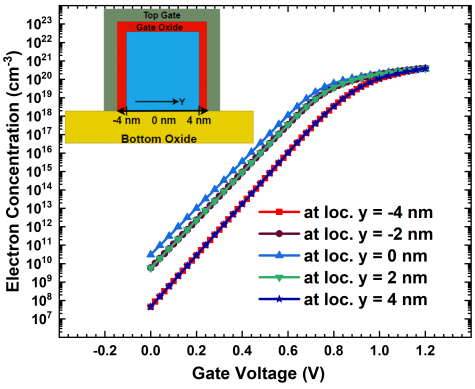


Fig. 5: Electron concentration versus gate voltage in the channel at various widths for $V_{ds} = 0.5$ V at $L_g/2$ (i.e. at X = 10 nm) and $H_{fin}/2$ (i.e. at Z = 6 nm).

potential in the channel under various gate voltages at different Y locations, potential plots were taken along a cutline in the X direction at Z = 6 nm as shown in figure 6. It can be observed that for all the gate voltages, the potential at Y = -4 nm is exactly the same as that of at Y = 4 nm throughout the length of the channel indicating the symmetry of the gate along the width of the channel. Hence for the gate biases below

the flatband condition conduction channel forms at the middle region of the channel (i.e. at $W_{fin}/2$) and the channel potential will be symmetrical along the width of the fin. It is evident in the figure 7 which is a potential contour plot in the XY plane at Z = 6 nm for V_g = 0.6 V that the potential is maximum at the middle of the width of the channel. At $V_g = 1.2$ V (i.e. at flatband condition), the entire channel along the width has the same potential. Hence the potential distribution at Y = -4 nm, 0 nm, and 4 nm are almost equal.

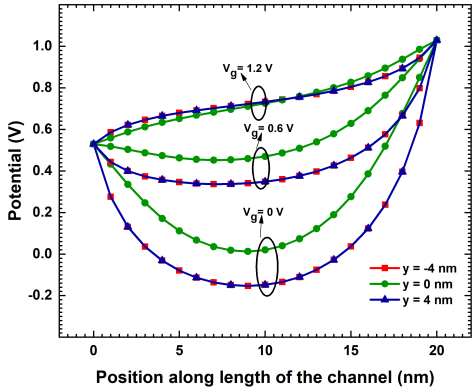


Fig. 6: Potential versus position along the length of the channel at various widths and various gate voltages for $V_{ds} = 0.5$ V at $H_{fin}/2$ (i.e. at Z = 6 nm).

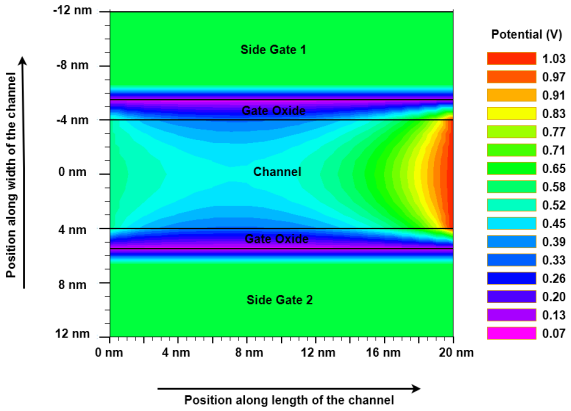


Fig. 7: Potential contour in XY plane at $V_g = 0.6$ V for $V_{ds} = 0.5$ V, at $H_{fin}/2$ (i.e. at Z = 6 nm).

B. Dependence of the Location of the EPCC on Transistor Structural Parameters

1) Impact of the Properties of Materials Constituting Gate as well as Gate Oxide on the Location of the EPCC: Figure 8 represents the location of the EPCC (i.e. maximum potential point) along the height of the channel versus gate voltage for different gate work functions at the centre of the width (i.e. at Y = 0 nm) and the middle of the length (i.e. at X = 10 nm) of the channel. It can be observed that as the gate work function increases maximum potential region in the channel shifts toward the BOX-channel interface. The work function difference between the gate and the silicon channel influences the depletion region formed in the channel. As the work function difference increases, the silicon channel will have more depletion. This impact will be more on the top and middle regions of the channel because of their proximity to the top gate. So, the bottom of the channel will be less depleted and have a higher electron concentration when the work function of the gate increase.

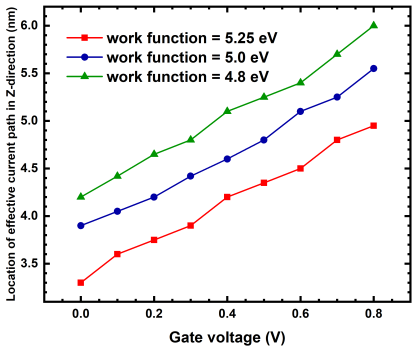


Fig. 8: Location of the effective current path along the height of the channel versus gate voltage for different gate work functions for $V_{ds} = 0.5$ V at $W_{fin}/2$ (i.e. at Y = 0 nm) and $L_g/2$ (i.e. at X = 10 nm).

Figure 9 represents the location of the EPCC along the height of the channel versus gate voltage for various gate oxide thicknesses at the centre of the width (i.e. at Y = 0 nm) and the middle of the length of the (i.e. at X = 10 nm). It can be observed that as the gate oxide thickness is decreased maximum potential region in the channel shifts towards the BOX-channel interface and away from the middle

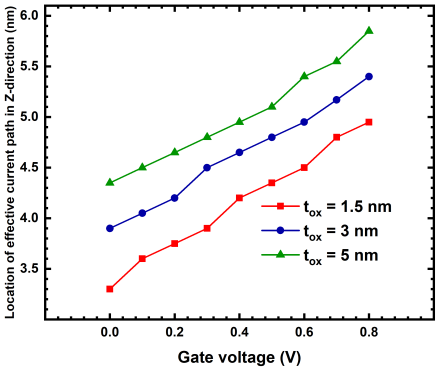


Fig. 9: Location of the effective current path along the height of the channel versus gate voltage for different gate oxide thicknesses for $V_{ds} = 0.5$ V at $W_{fin}/2$ (i.e. at Y = 0 nm) and $L_g/2$ (i.e. at X = 10 nm).

of the channel. As the gate oxide thickness decreases the gate oxide capacitance (C_{ox}) increases which increases the electric field lines passing into the channel. As electric field lines increase, the electrons which are majority carriers are pushed away from the gate surfaces [8]. Since the electrons are pushed away from gate surfaces the EPCC shifts towards the BOX-channel interface as oxide thickness is decreased.

Figure 10 represents the location of EPCC versus gate voltage for different gate oxide materials at the centre of the width (i.e. at Y = 0 nm) and middle of the length of the channel (i.e. at X = 10 nm). The gate oxide thickness of all the materials is kept the same which is 1.5 nm. The dielectric materials chosen for analysis are SiO_2, HfO_2, and TiO_2 which have dielectric constants of 3.9, 22, and 80 respectively. It can be observed that as the gate oxide material dielectric constant is increased (especially for high-K dielectrics like HfO_2, and TiO_2) EPCC in the channel shifts towards the BOX-channel interface. As the dielectric constant of the gate oxide increases, (C_{ox}) will increase resulting in stronger electric field lines from the gate into the channel. The increased electric field lines will force the electrons (majority carriers) to shift away from the gate surfaces [8]. Hence as the dielectric constant increases, the EPCC will shift towards the BOX-channel interface.

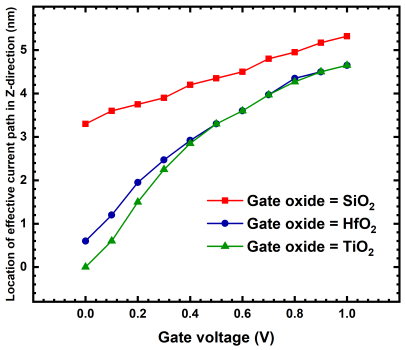


Fig. 10: Location of the effective current path along the height of the channel versus gate voltage for different gate oxide materials for $V_{ds} = 0.5$ V at $W_{fin}/2$ (i.e. at Y = 0 nm) and $L_g/2$ (i.e. at X = 10 nm).

2) Impact of the Channel Dimensions on the Location of the EPCC: Figure 11 represents the location of the EPCC along the height of the channel for different gate lengths at the middle of the width of the fin (i.e. at Y = 0 nm) and middle of the length of the channel. It can be observed that when the device is in full depletion mode (i.e. when $V_g < 0.75$ V) the device with longer length has the EPCC near BOX-channel interface, as the length decreases the EPCC keeps shifting towards the middle of the channel. This phenomenon can be attributed to the fact that when the device has a longer length, the location of $L_g/2$ will be far from the drain terminal of the device. So the influence of drain bias is less on the longer channel devices and hence the influence of drain bias in depleting the BOX-channel interface decreases, therefore the EPCC will be near the BOX-channel interface. However, when the device is in partial depletion mode (i.e. when $V_g > 0.75$ V), the effect of gate bias surpasses the effect of drain bias and hence the three plots converge as shown in the figure 11.

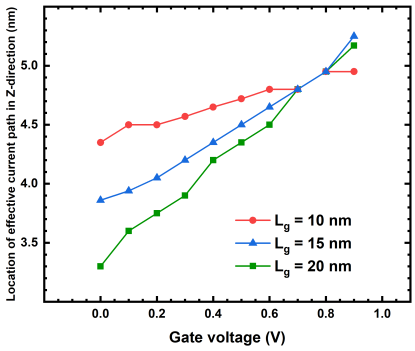


Fig. 11: Location of the effective current path along the height of the channel versus gate voltage for different gate lengths for $V_{ds} = 0.5$ V at $W_{fin}/2$ (i.e. at Y = 0 nm) and $L_g/2$ (i.e. at X = 0 nm).

Figure 12 represents the location of the EPCC along the height of the channel versus gate voltage for different widths of the fin at the centre of the channel (i.e. at y = 0 nm and x = 10 nm). It can be observed that as the width of the device is decreasing, the maximum potential region is shifting away from the BOX-channel interface. This is because when the width is less the side gates' electric field becomes dominant resulting in an effective depletion of the channel at the BOX-channel interface. As the width of the channel increases the electric field coupling between the side gates becomes weak resulting in faster uncovering of the depletion region near the BOX-

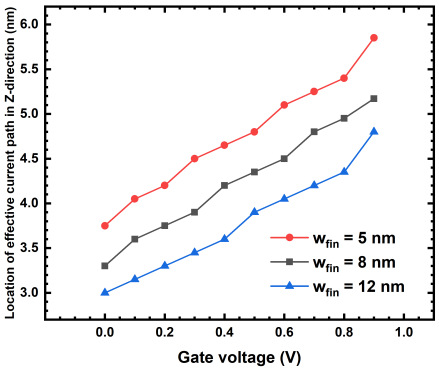
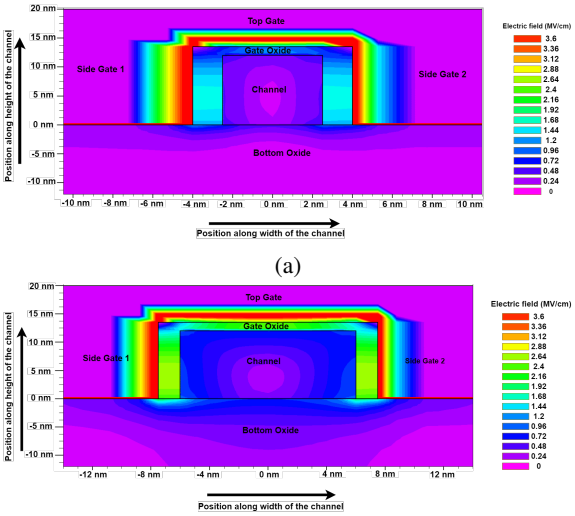


Fig. 12: Location of the effective current path along the height of the channel versus gate voltage for different widths of the fin for $V_{ds} = 0.5$ V at $W_{fin}/2$ (i.e. at Y = 0 nm) and $L_g/2$ (i.e. at X = 10 nm).

channel interface hence EPCC approaches the BOX-channel interface with an increase in fin width. A close inspection of figure 13 which portrays the electric field contours in the YZ plane at X = 10 nm for V_{ds} = 0.5 V, V_g = 0.4 V, reveals that when $W_{fin} = 5nm$ the strength of electric field lines is weak in the top gate oxide whereas when $W_{fin} = 12$ nm, the weaker electric field is confined only to the side corners of the top gate oxide which proves the dependence of electric field coupling on the width of the fin.



(a)

(b)

Fig. 13: Electric field contours in YZ plane for V_d = 0.5 V, V_g = 0.4 V at $L_g/2$ for (a) $W_{fin} = 5$ nm (b) $W_{fin} = 12$ nm

Figure 14 represents the position of the EPCC along the height of the channel versus gate voltage for different heights of the fin at the centre of the channel (i.e. at Y = 0 nm and at X = 10 nm). It can be observed that as the height of the fin is decreasing, the EPCC is shifting towards the BOX-channel interface. When the height of the fin is less, the top gate along with the side gates effectively depletes much of the channel region near these gates forcing the EPCC to shift towards the BOX-channel interface. However, as the height of the fin increases the top gate's influence on the channel subsides due to the increased distance between the top gate and middle region whereas capacitive coupling between side gates dominates in depleting the channel region near the BOX-channel interface. This results in an EPCC to shift towards the middle of the channel region.

IV. Conclusion

The electron concentration and potential distributions in the channel at various locations of the fin for n-type TG SOI JLFinFET to determine the location of the EPCC were studied. It is observed that while the device is transitioning from the OFF state to the ON state the EPCC will be near the middle of the channel along the height (i.e. $H_{fin}/2$) and the width (i.e. $W_{fin}/2$) for the simulated device. The dependence of the location of the EPCC on various structural parameters of

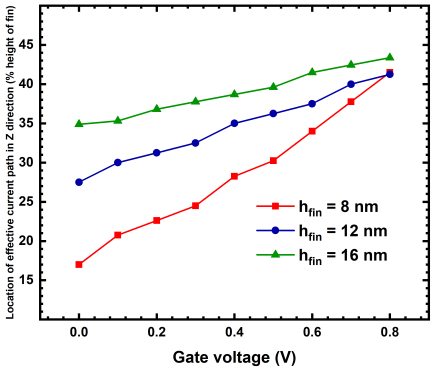


Fig. 14: Location of the effective current path along the height of the channel versus gate voltage for different heights of the fin for V_{ds} = 0.5 V at $W_{fin}/2$ (i.e. at Y = 0 nm) and $L_g/2$ (i.e. at X = 10 nm).

the transistor is also studied. The variation in C_{ox}, capacitive coupling effect play a major role in determining the location of the EPCC. It is observed that as the gate work function, gate oxide dielectric constant, length of the channel, and width of the channel increase the EPCC shifts towards the BOX-channel interface. When the gate oxide thickness and height of the channel increase the EPCC will shift away from the BOX-channel interface. The investigation into the impact of transistor structural parameters on the location of EPCC in JLFET has not been previously explored. This study represents the first attempt to analyze this relationship. The formation of EPCC in the middle of the channel could have advantages over conduction at the BOX-channel interface which are yet to be explored.

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