A nW Sub 1-Volt MOSFET-only Voltage Reference with a 32 ppm/°C Temperature Coefficient and 0.648V Power Supply

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***Abstract*—Voltage references are crucial for various mixed-signal and RF systems in the analog market, including IoT, wireless technologies, and body-area networks. In recent technological advancements, the increasing demand for low-power, low-cost, and energy-efficient solutions has driven the need for sub-1V voltage reference circuits. This paper presents the design and development of a sub 1-V voltage reference circuit for ultra-low power applications.The MOSFET-only circuit proposed here is compatible with CMOS fabrication in the 180 nm node. The voltage reference circuit achieves a stable 0.406V reference with a low line sensitivity (LS) of only 0.2%/V over a wide source voltage range from 648mV to 3.6V. It exhibits a temperature coefficient (TC) of 32 ppm/°C within the temperature range of -40°C to 105°C with a power consumption of 9.9nW at room temperature. The performance analysis includes a comprehensive assessment considering all process corners and statistical analysis through Monte Carlo simulations. Furthermore, a comparison with state-of-the-art references validates the effectiveness of the proposed circuit.**

***Index Terms*—Sub 1-Volt, Ultra low power, Voltage Reference, Line Sensitivty, Temperature Coefficient, PSRR, Monte-Carlo simulations**

I. Introduction

The expansion of Internet of Things (IoT) has increased the demand for ultra-low-power gadgets that can run for extended periods on battery power. The influence of the IoT on various applications, including business, healthcare, home automation, and transportation, has generated much attention. Sub-1-volt voltage reference circuits have become an important field of research to achieve this. These circuits give precise voltage references while requiring little power, making them perfect for Internet of Things applications. For a battery to last longer, low-power chips are required. The sub-threshold CMOS voltage reference has become well-known due to its low-power operation among the many voltage reference topologies. The need for accurate voltage references under severe energy restrictions has drawn much research attention due to the rise of wireless sensor networks and mobile devices. Modern SoC applications depend heavily on ultra-low-power voltage reference circuitry. In the recent literature, advances in voltage reference circuits have been reported [1]- [8].

Voltage references (VRs) are crucial for numerous electrical systems, including test and high-precision instrumentation. A complementary-to-absolute-temperature(CTAT) voltage and a proportional-to-absolute-temperature(PTAT) voltage can be scaled and added to create a temperature-independent reference voltage [2]. Banba et al. [9] have used bipolar junction transistors (BJTs) to constitute a bandgap reference (BGR) circuit. Though the circuit mentioned above could achieve a small temperature coefficient, the BGRs are not competitive regarding the minimum supply voltage. The resistors in BGRs make it difficult to decrease power consumption without significantly expanding the surface area. The methods proposed in [3], [7], and [8] avoid the use of resistors and BJTs and hence, achieve compact ultra low power VRs but with poor temperature stability [TCs $>$ 70 ppm]. The literature shows that MOSFET-only reference [1]– [8] operates with relatively lower power consumption.

This paper presents a CMOS Voltage Reference (CVR) circuit that uses no amplifiers or passive components to drastically reduce the temperature coefficient of the reference voltage to supply voltage. This study gives an overview of the numerous voltage reference topologies, their features, and the strategies used to increase accuracy and reduce power usage. It also highlights some of the significant issues in constructing sub-1 volt voltage reference circuits and make recommendations for future research.

This paper is arranged as follows. Section II presents the principle of operation of the designed voltage reference circuit with the circuit diagram and and design considerations. The simulation results and discussions are presented in Section III. Section IV

concludes this paper.

II. Principle of Operation

This section presents the design considerations for creating a voltage reference circuit that operates at extremely low power while maintaining a low average temperature coefficient. A CMOS voltage reference circuit is introduced, which operates with extremely low power consumption. Despite utilizing a sub-1V supply voltage, this circuit generates a stable output reference voltage.

The reference voltage is obtained by combining the CTAT and PTAT voltages [10]. By summing the CTAT and PTAT voltages, the resulting V_{REF} represents a combination of temperature-dependent and temperature-independent components, leading to a stable output voltage.

The difference in the gate-to-source voltages of two NMOS transistors, NM2 and NM3, in the circuit yields the CTAT component of the voltage reference. By carefully designing and configuring the two NMOS transistors in the circuit(with the size of NM3 greater than that of NM2), their V_{GS} values can be utilized to generate a voltage that is complementary to the absolute temperature. This means that as the temperature increases, the CTAT voltage decreases, and vice versa.

By measuring the difference in V_{GS} between these transistors, the circuit can extract the CTAT component contributing to the overall reference voltage. In addition to the CTAT contribution obtained from the difference in V_{GS} of the two NMOS transistors, the negative feedback mechanism in the circuit also contributes to the CTAT part of the output voltage.

The negative feedback in the circuit is intended to keep the output voltage accurate and stable. Based on the discrepancy between the required reference voltage and the actual output voltage, it modifies the transistors' operating conditions. This feedback mechanism plays a role in compensating for temperature variations and ensuring that the output voltage remains relatively stable over a range of temperatures. The feedback loop monitors the output voltage and makes the necessary adjustments to the circuit parameters, such as biasing currents or voltages to counteract temperature-induced changes.

In the proposed circuit, the PTAT part of the output reference voltage is generated by utilizing the voltage drop across a diode-connected PMOS transistor.

The voltage drop across the transistor is approximately linearly proportional to the absolute temperature. By carefully selecting the biasing conditions and the transistor parameters, such as the width (W) and length (L) of the transistors, the voltage drop across the diode-connected PMOS transistor can be made to exhibit a PTAT behavior when the bias current I6 is the near-cutoff current of PM6. This means that the voltage drop changes in a predictable and proportional manner with variations in temperature.

The PTAT voltage is then combined with the CTAT component resulting in the overall output reference voltage, V_{REF}.

In this paper, we adopt the circuit design in [7]

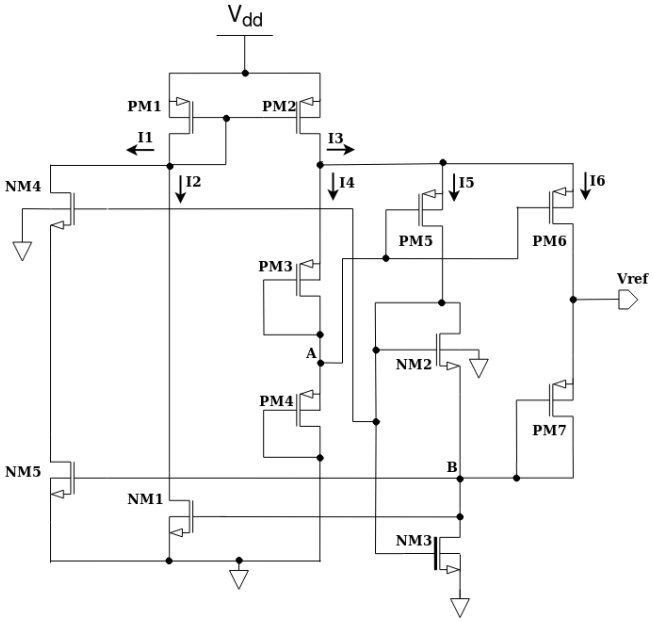

Fig. 1. Schematic diagram of the Circuit

as the foundation for our current generator part. The motivation behind this choice stems from the circuit's remarkable features and advantages. Line Sensitivity (LS) has been significantly reduced in the design. Ultra-low power consumption is made possible by operating all transistors in the subthreshold region, making it ideally suited for IoT applications with limited power. The circuit construction is made simpler by the lack of amplifiers or passive components, which results in a smaller chip area and more effective implementation. Our present generator design exhibits the potential for improved performance and efficiency in the chosen application sector by utilizing these attractive qualities.

In the circuit, MOSFETs PM1 to PM4 and NM1 collectively form the current generator component [7].In contrast to the reference paper's current generator design, we have made an enhancement by introducing an additional diode-connected PMOS (PM4) to improve the LS of the circuit. This current generator is responsible for providing a stable and well-controlled current that is utilized in biasing the circuit. By selecting the appropriate transistor sizes, biasing conditions, and ensuring proper matching and temperature compensation, the current generator based on MOSFETs PM1 to PM4 and NM1 achieves the desired performance in terms of current accuracy, temperature stability, and low-power operation.

By connecting PM3 and PM4 as a diode, it creates a

low-impedance path to ground at point A in the circuit to diminish the sensitivity of V_A to V_{DD}. The voltage at point A is frequently impacted by these fluctuations when the V_{DD} varies. However, due to the presence of the diode-connected PM3 and PM4 and the low-impedance path it establishes, the sensitivity of V_A to V_{DD} is reduced. This indicates that the voltage at point A is relatively stable even when V_{DD} varies. The stability of V_A is crucial because it impacts the overall performance of the circuit, particularly the stability of the reference voltage .This stable V_{REF} helps to minimize the impact of changes in the power supply voltage on the circuit's functionality (Fig.2).

$$LS = \frac{\Delta V_{\text{ref}}}{\Delta V_{\text{DD}}} \cdot \frac{1}{V_{\text{ref}}} \cdot 100\% \quad (1)$$

To reduce the TC, we have introduced MOSFETs NM4 and NM5 in the circuit [10]. In the circuit, when the temperature increases, the currents I5 and I6 also increase. The current I5 flows through transistors NM2 and NM3, and the voltage at point B is determined by the difference in gate-to-source voltages of NM3 and NM2. The sizing of NM2 and NM3 is such that NM3 has a very high threshold voltage and is larger than NM2.

As a result, when the current I5 increases, the gate-to-source voltages of NM2 and NM3 need to adjust to reflect this change. However, since NM3 is larger in size compared to NM2, the change in gate-to-source voltage of NM3 is very small, while the change in NM2 is significant. This further decreases the voltage at point B, which is the same as the gate-to-source voltage of NM5.

Because NM5 is less biased compared to NM4, NM4 can handle current changes in the circuit better than NM5. This leads to a reduction in the voltage drop across NM5 and subsequently decreases the currents I1 and I2. The current mirrors PM1 and PM2 further reduce the currents I4 and I3. Consequently, the values of currents I5 and I6 decrease.

In conclusion, the feedback network in this circuit provides compensation, stabilizing the voltage and current at the output. This helps reduce the temperature coefficient (TC) value. Optimum adjustments of the current throughout the circuit enable high-temperature compensation.

MOSFETs PM5 and PM6 in the circuit are working near cut-off region and hence the currents I5 and I6 are reverse saturation currents. The voltage across a diode connected transistor is given by the equation

$$V = V_T \ln\left(\frac{I_D}{I_F}\right)$$

where V_T is the thermal voltage, I_D is the drain current and I_F is the forward saturation current.

Here, I_D is the reverse saturation current I6. Therefore, I_D and I_F gets cancelled and voltage drop across PM7 becomes the thermal voltage V_T ($V_T = \frac{kT}{q}$). Aside from the norm, we have made the voltage drop across the diode connected transistor PM7 a PTAT voltage.

Fig.1 displays the schematic of the temperature compensated voltage reference. It consists of a current generator part, whose current, is delivered to an active load which provides the temperature compensated reference voltage, V_{REF} as output. The sub-threshold current for an NMOS transistor, I_{sub} is given by

$$I_{sub} = \mu C_{OX} k(\eta - 1) V_T^2 exp\left(\frac{V_{GS} - V_{th}}{\eta V_T}\right) \quad (2)$$

The sub-threshold current for an PMOS transistor, I_{sub} is given by

$$I_{sub} = \mu C_{OX} k(\eta - 1) V_T^2 exp\left(\frac{V_{th} - V_{GS}}{\eta V_T}\right) \quad (3)$$

where C_{OX} is the oxide capacitance per unit area, k is the W/L ratio of the transistor, V_T is the thermal voltage, μ is the mobility, η is the subthreshold slope parameter, V_{GS} is the gate-to-source voltage and V_{th} is the threshold voltage. Thereby gate-source voltage of an NMOS transistor, V_{GS} from (2) can be given by

$$V_{GS} = V_{th} + \eta V_T ln\left(\frac{I_{sub}}{kI_0}\right) \quad (4)$$

The gate-source voltage of an PMOS transistor, V_{GS} from (3) can be given by

$$V_{GS} = V_{th} - \eta V_T ln\left(\frac{I_{sub}}{kI_0}\right) \quad (5)$$

where parameter I_0 stands for $I_0 = \mu C_{OX}(\eta - 1){V_T}^2$. As apparent from Fig. 1, V_{REF} is given by

$$\begin{aligned} V_{REF} &= (V_{GS})_{PM7} + (V_{DS})_{NM3} \\ &= (V_{GS})_{PM7} + (V_{GS})_{NM3} - (V_{GS})_{NM2} \end{aligned} \quad (6)$$

As the transistors NM2, NM3, and PM7 are operating in subthreshold, with a bias current set to I_R. Using (4), (6) can be re-written as follows

$$\begin{aligned} V_{REF} &= (V_{th})_{NM3} - (V_{th})_{NM2} \\ &+ (V_{GS})_{PM7} + \eta V_T ln\left(\frac{k_{NM2}}{k_{NM3}}\right) \\ &= (V_{th})_{PM7} + (V_{th})_{NM3} - (V_{th})_{NM2} \\ &+ V_T ln\left(\frac{I_R k_{PM7}}{I_0}\right) + V_T ln\left(\frac{k_{NM2}}{k_{NM3}}\right) \end{aligned} \quad (7)$$

Therefore, V_{REF} turns out to be the weighted combination of terms that exhibit opposite temperature dependence: thermal voltage V_T, which has a positive temperature coefficient (TC), and threshold voltage V_{th}, which has a negative TC. As a result, the TC of V_{REF} can be expressed as

$$\frac{\delta V_{REF}}{\delta T} = -\frac{|k_{th}|}{T_0} + \eta \frac{K_B}{q} ln\left(\frac{I_R k_{PM7} k_{NM2}}{I_0 k_{NM3}}\right) \quad (8)$$

where k_{th} is given as $k_{th} = \delta V_{th}/\delta T$, T_0 is the absolute temperature, η is the subthreshold slope parameter, K_B is the Boltzmann constant, q is the electric charge, k_i is the W/L ratio of the $M_i - th$ transistor. From (8), the relation between TC and I_R can be easily depicted. So by finding an optimum value of (W/L) ratio of transistors PM5 and PM6, we have tried to decrease the current I_R, and thereby decrease the dependence of V_{REF} with respect to temperature. This aids in a drastic decrease in TC at room temperature. The schematic of the voltage reference is shown in Fig. 1 with transistors PM1 - PM7 being PMOS and NM3 being a thick oxide NMOS whereas NM1, NM2, NM4, and NM5 are NMOS transistors. The (W/L) ratios of the transistors are reported in Table I. Optimum values for W and L for transistors were taken after performing the parametric analysis with respect to temperature and supply voltage.

TABLE I
TRANSISTOR SIZES[W/L]

Transistor	Circuit 2
PM1	12µm/4µm
PM2	24µm/4µm
PM3	2µm/180nm
PM4	400nm/18µm
PM5	40µm/1µm
PM6	5µm/3µm
PM7	400nm/3µm
NM1	24µm/4µm
NM2	15µm/17µm
NM3	25.3µm/40µm
NM4	1µm/20µm
NM5	30µm/20µm

III. RESULTS AND DISCUSSION

Simulations are run on the Cadence Virtuoso Platform to analyze the performance parameters. It makes use of the UMC process development kit for the 180 nm node. Table I gives the transistor sizing. All potential process corners are taken into account. To evaluate the fluctuations in performance characteristics of circuits in the actual fabrication environment, statistical analysis based on Monte Carlo simulation is used. The performance parameters of our work are compared with the recent works on the topic. The output reference voltage is plotted as a function of the supply voltage in Fig.2. The LS calculated at a nominal temperature of 27^{o}C is 0.2%/V. The variation of output voltage with temperature from -40 to 105^{o}C at different operating voltages are shown in Fig.3.

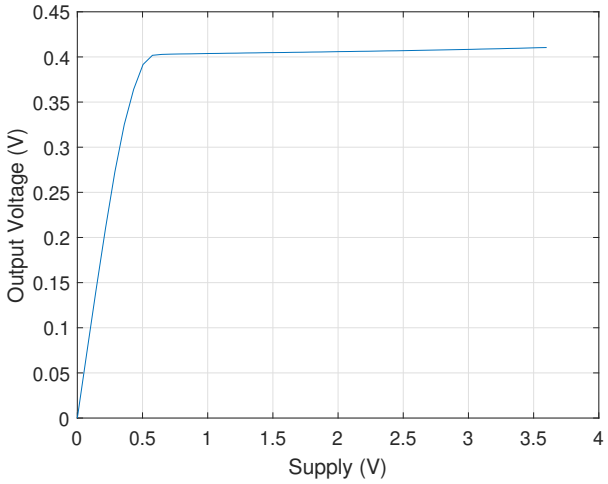

Fig. 2. Plot of output voltage with supply voltage

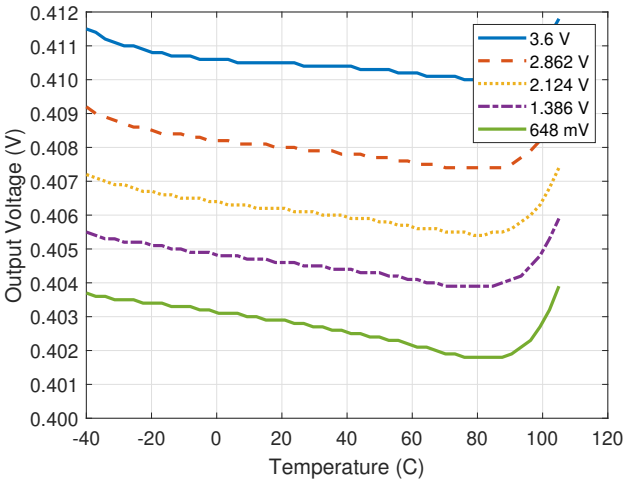

Fig. 3. Plot of output voltage with temperature at five supply voltages

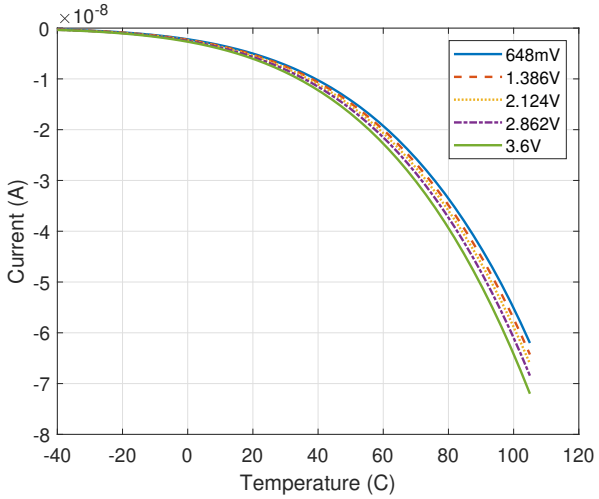

Fig. 4. Plot of supply current with temperature at different supply voltages

The TC at a nominal supply voltage of 648mV is obtained as 32ppm/^{o}C. The values of the Temperature Coefficient obtained after 200 runs of Monte-Carlo simulation can be seen as a histogram in Fig.6, with a mean value of μ = 39.999ppm/^oC and standard deviation of σ = 8.892ppm/^oC. The results indicate that very good temperature compensation is achieved; thus, a low TC could be achieved. The power consumed by the circuit at 27^{o}C is 9.9nW. From Fig.5, PSRR of -17.4dB is obtained at 10MHz without the use of a capacitor, and a high PSRR of about -52.6dB is obtained at 10MHz with the use of a capacitor at the output point. The key performance parameters of the proposed circuit, as well as those of state-of-the-art references, are presented in Table II for comparison.

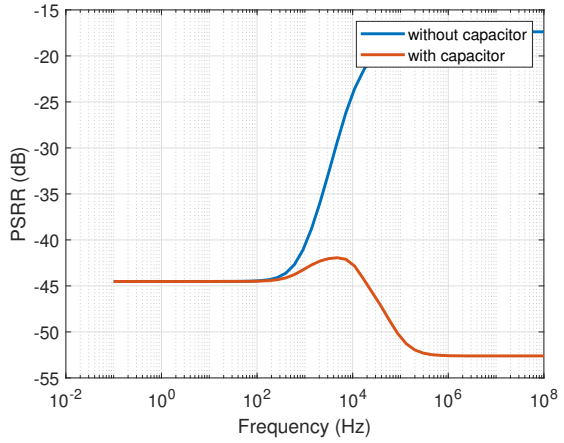

Fig. 5. Comparison plot of PSRR - with and without capacitor

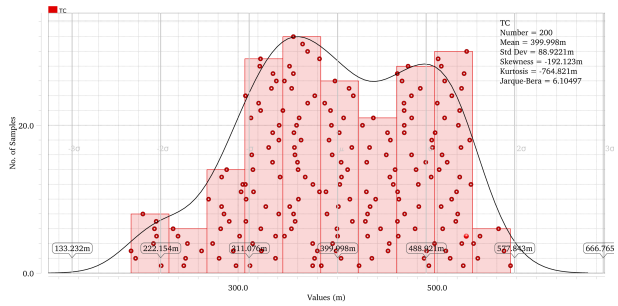

Fig. 6. Monte-Carlo plot of temperature coefficient

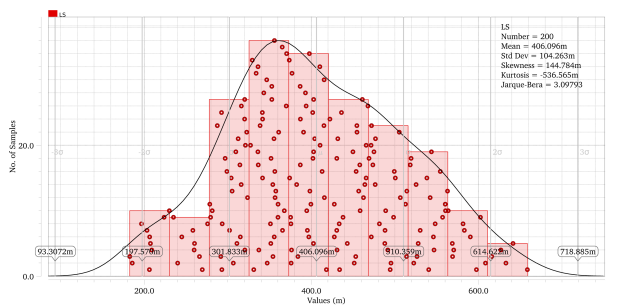

Fig. 7. Monte-Carlo plot of nominal output voltage

IV. Conclusion

A low-power voltage reference circuit with low-temperature coefficient while conserving silicon area is implemented using 0.18μm CMOS process. The achieved temperature coefficient of 32 ppm/^{o}C in a wide temperature range, sub-1 V reference voltage, and excellent PSRRs with filter capacitor make this circuit suitable for various applications, especially those that require low power consumption. Additionally, the statistical analysis based on Monte Carlo simulation indicates that the circuit's performance is robust against process variations. The low power consumption of 9.9 nW and compact active area of 0.002785 mm^2 further enhance the circuit's practicality and cost-effectiveness. Overall, the presented voltage reference circuit is a promising solution for low-power applications that demand small area and stable performance over a wide range of operating conditions. These circuits can be used for applications such as wireless sensor nodes powered by energy harvesting and implantable medical devices.

V. Acknowledgement

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TABLE II
COMPARISON TABLE

Work	Year	Technology	Supply voltage	TC (ppm/^oC)	Temp.range	LS (%/V)	PSRR(dB) @ 27^oC	Power	Area(mm^2)	V_{ref}
[1]	2018	0.13µm	1.1V	best - 30 mean - 100 worst - 450	-40,80	2	-36dB		0.003	0.800V
[2]	2018	0.18µm	2V	32.7 at -45^oC 89 at 125^oC	-45,125	0.058	-85dB @100Hz	192nW	0.063	1.2V
[3]	2017	0.18µm	0.4V	82	-40,140	0.027	-59dB @ 10Hz -47dB @ 1KHx -53dB @ 1MHz	9.6nW	0.021	0.210V
[4]	2011	0.13µm	1.2V	48	0,100	2.655	-51.4dB @ 100Hz	-	0.0533	0.781V
[5]	2018	0.18µm	1.1V	20 - min 34 - typical 89 - max	-15,140	0.28	-9 @ 10Hz	4.6nW	0.0598	0.755V
[6]	2019	0.13µm	1V	35	-25,85	0.15	-50 @ 100Hz	20 pW	0.003	0.560V
[7]	2019	0.18µm	0.4V	89.83	-40,125	0.0154	-73dB @ 10Hz	1nW	0.005	0.151V
[8]	2021	0.18µm	0.25V	73.5	-40,140	0.3	-65dB @ 100Hz	119pW	0.0009	0.1181V
[10]	2019	0.18µm	0.95V	88	-20,80	0.073	-41dB @ 100Hz	2.4nW	0.03155	0.773V
[11]	2019	0.18µm	1.2V	780	0,80	0.58	-41dB @ 100Hz	23pW	0.3820	0.27V
This Work	2023	0.18µm	648mV	**32**	**-40,105**	0.2	-44.4dB @ 100Hz	**9.9nW**	**0.002**	0.406V

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